Detailed Joint GLSVLSI and MSE Program

GLSVLSI 2017

May 10 – 12

Lake Louise, Canada

MSE 2017

May 11 – 12

Lake Louise, Canada

Wednesday, May 10, 2017

<table>
<tr><td>9:00 – 10:00</td><td colspan="2">Keynote 1 - MT Temple A
Leland Chang, Senior manager VLSI Design, IBM Research
<u>Cognitive Data-centric Systems</u>
Moderator: Deming Chen, University of Illinois at Urbana-Champaign, USA</td></tr>
<tr><td>10:00 – 10:20</td><td colspan="2">Coffee Break - Trails Foyer</td></tr>
<tr><td>10:20 – 12:00</td><td><u>Session 1</u><u>: Emerging Technologies and Paradigms for Low Power Computing</u> - Lakeshore
Session Chairs
Deliang Fan, University of Central Florida, USA (Chair)
Deming Chen, University of Illinois at Urbana-Champaign, USA (Co-Chair)

1) Design of a Low-Power Non-Volatile Programmable Inverter Cell for COGRE-based Circuits, Fabrizio Lombardi, Pilin Junsangsri, Salin Junsangsri and Martin Margala
2) VaLHALLA: Variable Latency History Aware Local-carry Lazy Adder, Ali Murat Gok and Nikos Hardavellas
3) Energy Efficient Magnetic Tunnel Junction Based Hybrid LSI Using Multi-Threshold UTBB-FD-SOI Device, Hao Cai, You Wang, Lirida Naviner, Wang Kang and Weisheng Zhao
4) A Mixed-Size Monolithic 3D Placer with 2D Layout Inheritance, Xu He, Yao Wang, Yang Guo and Sorin Cotofana
5) *LightNN: Filling the Gap between Conventional Deep Neural Networks and Binarized Networks (Best Paper Candidate), Ruizhou Ding, Zeye Liu, Rongye Shi, Diana Marculescu and Shawn Blanton</td><td><u>Session 2:</u><u> Design Techniques for Non-Traditional Computing</u> - Beehive
Session Chairs
Wujie Wen, Florida International University, USA (Chair)
Gang Qu, University of Maryland, USA (Co-Chair)

1) Design of a Flash-based Circuit for Multi-Valued Logic, Monther Abusultan and Sunil Khatri
2) Design of Approximate Logarithmic Multipliers, Weiqiang Liu, Jiahua Xu, Danye Wang and Fabrizio Lombardi
3) Mitigating the Effect of the Reliability Soft-errors of the RRAM Devices on the Performance of the RRAM-based Neuromorphic Systems, Amr Tosson, Shimeng Yu, Mohab Anis and Lan Wei
4) A Spin Transfer Torque based Cellular Neural Network (CNN) Architecture, Yu Bai
5) Neuro-NoC: Neural Network based Predictive Routing for Network-on-Chip Architectures, Michel Kinsy and Shreeya Khadka</td></tr>
<tr><td>12:00 – 1:30</td><td colspan="2">Lunch
MT Temple A</td></tr>
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<td>1:30 – 2:50</td>
<td>Session 3: Strategies for In-Memory Computing - Lakeshore
Session Chairs
Jie Han, University of Alberta, Canada (Chair)
Miroslav Velev, Aries Design Automation, USA (Co-Chair)

1) *A Domain-Specific Language and Compiler for Computation-in-Memory Skeletons (Best Paper Candidate), Jintao Yu, Tom Hogervorst and Razvan Nane
2) Energy Efficient In-Memory Computing Platform Based on 4-Terminal Spin Hall Effect-Driven Domain Wall Motion Devices, Shaahin Angizi, Zhezhi He and Deliang Fan
3) Leveraging Dual-Mode Magnetic Crossbar for Ultra-low Energy In-Memory Data Encryption, Zhezhi He, Shaahin Angizi, Farhana Parveen and Deliang Fan
4) Evaluating Data Resilience in CNNs from an Approximate Memory Perspective, Yuanchang Chen, Yizhe Zhu, Fei Qiao, Jie Han, Yuansheng Liu and Huazhong Yang</td>
<td>Special Session 1: Low Power Computing based on Non-Volatile Memories - Beehive
Session Chairs
Weisheng Zhao, Beihang University (Chair)
Damien Querlioz, University of Paris Saclay, CNRS (Co-Chair)

1) Advanced Low Power Spintronic Memories beyond STT-MRAM, Wang Kang, Zhaohao Wang, He Zhang, Sai Li, Youguang Zhang and Weisheng Zhao
2) Exploiting Non-Volatility for Information Processing, Robert Perricone, Li Tang, X. Sharon Hu and Michael Niemier
3) Neuromorphic Computing Based on Resistive RAM, Zixuan Chen, Huaqiang Wu, Bin Gao, Peng Yao, Xinyi Li and He Qian
4) Implications of the Use of Magnetic Tunnel Junctions as Synapses in Neuromorphic Systems, Adrien F. Vincent, Nicolas Locatelli, Qifan Wu and Damien Querlioz
5) Bio-inspired Programming of Resistive Memory Devices for Implementing Spiking Neural Networks, Elisa Vianello, Thilo Werner, Olivier Bichler, Etienne Nowak, Alessandro Grossi, Blaise Yvert, Barbara De Salvo, and Luca Perniola
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<tr>
<td>2:50 – 3:50</td>
<td colspan="2">Poster Session 1 - CAD, VLSI Design, VLSI Circuits and Power Aware Design - MT Temple A

1) A maze routing-based algorithm for ML-OARST with pre-selecting and ripping up and re-building Steiner points, Kuen-Wey Lin, Yeh-Sheng Lin, Yih-Lang Li and Rung-Bin Lin
2) An Integrated Optimization Framework for Partitioning, Scheduling and Floorplanning on Partially Dynamically Reconfigurable FPGAs, Xiaodong Xu, Qi Xu, Jinglei Huang and Song Chen
3) Communication-aware Partitioning for Energy Optimization of Large FPGA Designs, Kalindu Herath, Alok Prakash, Jiang Guiyuan and Thambipillai Srikanthan
4) Combined Centralized and Distributed Connection Allocation in Large TDM Circuit Switching NoCs, Yong Chen, Emil Matus and Gerhard Fettweis
5) Random Forest Architectures on FPGA for Multiple Applications, Xiang Lin, Shawn Blanton and Donald Thomas
6) Exploring Heterogeneous-ISA Core Architectures for High-Performance and Energy-Efficient Mobile SoCs, Wooseok Lee, Dam Sunwoo, Christopher D. Emmons, Andreas Gerstlauer and Lizy John
7) An FPGA Coarse Grained Intermediate Fabric for Regular Expression Search, Thomas Luinaud, Pierre Langlois and Yvon Savaria
8) Deadline-Aware Joint Optimization of Sleep Transistor and Supply Voltage for FinFET Based Embedded Systems, Huimei Cheng, Ji Li, Jeffrey Draper, Shahin Nazarian and Yanzhi Wang</td>
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	9) Energy Savings and Performance Improvement in Subthreshold Using Adaptive Body Bias, *Rajsaktish Sankaranarayanan and Matthew R. Guthaus* 10) Low voltage stochastic flash ADC with front-end of inverter-based comparative unit, *Xuncheng Zou, Bo Liu and Shigetoshi Nakatake*	
3:50 – 5:30	**Session 4:** Circuits, Architectures, and System Level Issues for Many-Core Processors – *Lakeshore* Session Chairs: Lombardi Fabrizio, Northeastern University, USA (Chair) Ioannis Savidis, Drexel University, USA (Co-Chair) 1) *A Robust C-element Design with Enhanced Metastability Performance (Best Paper Candidate), *Kinshuk Sharma and Sunil Khatri* 2) Circuit Level Design of a Hardware Hash Unit for use in Modern Microprocessors, *Abbas Fairouz, Monther Abusultan and Sunil Khatri* 3) DELCA: DVFS Efficient Low Cost Multicore Architecture, *Shoumik Maiti and Sudeep Pasricha* 4) EEAL: Processors' Performance Enhancement Through Early Execution of Aliased Loads, *Abhishek Rajgadia, Newton Singh and Virendra Singh* 5) Performance-aware resource management of multi-threaded applications on many-core systems, *Daniel Olsen and Iraklis Anagnostopoulos*	**Session 5:** CAD for the Nano Era - *Beehive* Session Chairs Weichen Liu, Chongqing University, China (Chair) Qiaoyan Yu, University of New Hampshire, USA (Co-Chair) 1) Redundant Via Insertion with Cut Optimization for Self-Aligned Double Patterning, *Youngsoo Song, Jinwook Jung and Youngsoo Shin* 2) Improving Circuit Mapping Performance Through MIG-based Synthesis for Carry Chains, *Zhufei Chu, Xifan Tang, Mathias Soeken, Ana Petkovska, Grace Zgheib, Luca Amaru, Yinshui Xia, Paolo Ienne, Giovanni De Micheli and Pierre-Emmanuel Gaillardon* 3) *Under-the-cell Routing to Improve Manufacturability (Best Paper Candidate), *Àlex Vidal-Obiols, Jordi Cortadella and Jordi Petit* 4) Boolean Decomposition for AIG optimization, *Lucas Machado and Jordi Cortadella* 5) Mixed-Cell-Height Standard Cell Placement Legalization, *Chung-Yao Hung, Peng-Yi Chou and Wai-Kei Mak*

Thursday, May 11, 2017

9:00 – 10:00	**Keynote 2** - *MT Temple A* Professor Niraj K. Jha, Department of Electrical Engineering, Princeton University Internet of Medical Things, Moderator: Jie Han, University of Alberta, Canada		
10:00 – 10:20	**Coffee Break** - *Trails Foyer*		
10:20 – 12:00	**Session 6:** Hardware Security: New Advances in Timing Side Channel and Logic Obfuscation - *Lakeshore* Session Chairs Houman Homayoun, George Mason University, USA (Chair) Guru Venkataramani, George Washington University, USA (Co-Chair) 1) Covert Timing Channels Exploiting Non-Uniform Memory Access based Architectures, *Fan Yao, Guru Venkataramani and Milos Doroslovacki* 2) A Novel Side-channel Timing Attack on GPUs, *Zhen Hang Jiang, Yunsi Fei and David Kaeli* 3) *A Low-Cost Secure GPS Spoofing Detector Design for the Internet of Things Applications (Best Paper Candidate), *Md Tanvir Arafin, Dhananjay Anand and Gang Qu* 4) Cyclic Obfuscation for Creating SAT-Unresolvable Circuits, *Kaveh Shamsi, Meng Li, Travis Meade, Zheng Zhao, David Z. Pan and Yier Jin* 5) Double DIP: Re-Evaluating Security of Logic Encryption Algorithms, *Yuanqi Shen and Hai Zhou*	**Session 7:** Testing and Reliability- *Beehive* Session Chairs Chih-Tsun Huang, National Tsing Hua University, Taiwan (Chair) Hung-Pin (Charles) Wen, National Chiao Tung University, Taiwan (Co-Chair) 1) *Efficient Critical Path Selection Under a Probabilistic Delay Model (Best Paper Candidate), *Ahish Mysore Somashekar and Spyros Tragoudas* 2) Combining Restorability and Error Detection Ability for Effective Trace Signal Selection, *Binod Kumar, Ankit Jindal, Masahiro Fujita and Virendra Singh* 3) Radiation-Hardened Designs for Soft-Error-Rate Reduction by Delay-Adjustable D-Flip-Flops, *Yuwen Lin, Charles H.-P. Wen, Herming Chiueh* 4) Effective Mitigation of Radiation-induced Single Event Transient on Flash-based FPGAs, *Luca Sterpone, Sarah Azimi, Boyang Du, David Merodio Codinachs and Raoul Grimoldi* 5) Energy Efficient Adaptive Approach for Dependable Performance in the presence of Timing Interference, *Nikolaos Zompakis, Michail Noltsis, Dimitrios Rodopoulos, Francky Catthoor and Dimitrios Soudris*	**MS Session 1:** *Plain of Six Glaciers* Moderator: *Chris Miller,* Rose-Hulman Institute of Technology 1) Design Flows and Collateral for the ASAP7 7nm FinFET Predictive Process Design Kit, *Lawrence Clark, Vinay Vashishtha, David Harris, Sam Dietrich and Zunyan Wang* 2) WIP: Open-Source Standard Cell Characterization Process-flow on 45 nm (FreePDK45), 0.18 µm, 0.25 µm, 0.35 µm and 0.5 µm, *Rabin Thapa, Samira Ataei and James Stine* 3) SoC FPAA Immersed Junior Level Circuits Course, *Jennifer Hasler, Aishwarya Aishwarya and Sahil Shah* 4) Teaching Microelectronics at Olin College, *Bradley Minch* 5) Innovative practice in the French microelectronics education targeting the industrial needs, *Olivier Bonnaud and Laurent Fesquet.*

12:00 – 1:30	**Keynote 3** and **Lunch** - *MT Temple A* Andrew Putnam, Microsoft Research Technologies (MSR-T) lab FPGAs in Datacenter – Combining the Worlds of Hardware and Software Development, Moderator: Miroslav Velev, Aries Design Automation		
1:30 – 2:50	**Session 8:** Emerging Technologies, RF Circuits and Security Functions - *Lakeshore* Session Chairs Tsung-Yi Ho, National Tsing Hua University, Taiwan (Chair) Deliang Fan, University of Central Florida, USA (Co-Chair) 1) Design Automation for Paper Microfluidics with Passive Flow Substrates , *Joshua Potter, William Grover and Philip Brisk* 2) *Neuromorphic 3D Integrated Circuit: A Hybrid, Reliable and Energy Efficient Approach for Next Generation Computing (Best Paper Candidate), *Md Amimul Ehsan, Zhen Zhou and Yang Yi* 3) Method for Phase Noise Analysis of RF Circuits, *Dimo Martev, Sven Hampel and Ulf Schlichtmann* 4) Revealing On-chip Proprietary Security Functions with Scan Side Channel Based Reverse Engineering, *Leonid Azriel, Ran Ginosar and Avi Mendelson*	**Special Session 2:** Three-Dimensional Integrated Circuit (3D-IC) Security - *Beehive* Session Chair Qiaoyan Yu, University of New Hampshire (Chair) 1) Security Threats and Countermeasures in Three-Dimensional Integrated Circuits , *Jaya Dofe, Peng Gu, Dylan Stow, Qiaoyan Yu, Eren Kursun and Yuan Xie* 2) Impact of Power Distribution Network on Power Analysis Attacks in Three-Dimensional Integrated Circuits, *Jaya Dofe, Zhiming Zhang, Qiaoyan Yu, Chen Yan and Emre Salman* 3) The Need for Declarative Properties in Digital IC Security, *Mohamed El Massad, Frank Imeson, Siddharth Garg and Mahesh Tripunitara* 4) Securing Split Manufactured ICs with Wire Lifting Obfuscated Built-In Self-Authentication, *Qihang Shi, Kan Xiao, Domenic Forte and Mark Tehranipoor*	**MS Session 2:** Panel: VLSI – The Tall Thin Designer Looks at 40: The Past, Present, and Future of VLSI Design Education - *Plain of Six Glaciers* Moderator: *John Nestor, Layfayette College* Panelists: David Harris, Harvey Mudd College Jennifer Hasler, Georgia Tech Russ Pina, MOSIS James Stine, Oklahoma State University This panel will explore the past, present, and future of VLSI Design courses, reflecting on how the original courses impacted education and technology, how courses have evolved over time in response to changes in technology and design methods, and what we might expect in these courses in the future.
2:50 – 3:20	**Coffee Break** - *Trails Foyer*		

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<td>3:20 – 4:40</td>
<td>Special Session 3: Logic Obfuscation for IoT Security: A New Arms Race? - Lakeshore
Yier Jin, University of Central Florida (Chair)
Gang Qu, University of Maryland (Co-Chair)

1) An Empirical Study on Gate Camouflaging Methods Against Circuit Partition Attack, Xueyan Wang, Qiang Zhou, Yici Cai and Gang Qu
2) What to Lock? Functional and Parametric Locking, Muhammad Yasin, Abhrajit Sengupta, Benjamin Carrion Schafer, Yiorgos Makris, Ozgur Sinanoglu and Jeyavijayan Rajendran
3) Circuit Obfuscation and Oracle-guided Attacks: Who Can Prevail?, Kaveh Shamsi, Meng Li, Travis Meade, Zheng Zhao, David Z. Pan, and Yier Jin
4) Comparative Analysis of Hardware Obfuscation for IP Protection, Sarah Amir, Bicky Shakya, Domenic Forte, Mark Tehranipoor, and Swarup Bhunia</td>
<td>Industry Academia Workshop – MT Temple A

Laleh Behjat, University of Calgary, Canada (Chair)
Tina Hudson, Rose-Hulman University, USA (Co-Chair)

In this facilitated workshop, we will bring together industry leaders, experienced faculty and students to discuss industrial issues related to microelectronics education. At the beginning, sponsoring companies will have an opportunity to present their university relations programs and products in an interactive, small-group setting. Each company will have a faculty advocate that uses their programs and/or products. Participants will rotate to different companies through this part of the workshop. In the second half of this workshop, small groups will have a facilitated discussion about the changing role of education in preparing students for the new challenges facing industry. Once the discussions are over, there will be a sharing of the main ideas of each group on the themes. The workshop will close by compiling a set of recommendations and best practices.</td>
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<td>5:00 – 7:00</td>
<td colspan="2">Hike around Lake Louise Shore line
Or
Chateau Lake Louise Tour</td>
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<td>7:00 – 9:00</td>
<td colspan="2">Banquet, awards and Invited Talk – Victoria Ballroom
Invited speaker: Dr. Eric Donovan, Professor and Associate Dean Research and Graduate Education for the University of Calgary, Faculty of Science
S.T.E.V.E. - The Best Backronym Ever!
Studying Aurora and the role of citizen scientists</td>
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Friday, May 12, 2017

9:00 – 10:00	**Keynote 4** - *MT Temple A* Alex Jones, Professor, University of Pittsburgh, Green Computing: New Challenges and Opportunities, Moderator: Laleh Behjat, University of Calgary, Canada		
10:00 – 10:20	**Coffee Break** - *Trails Foyer*		
10:20 – 12:00	**Session 9:** CAD under Challenges: Tight Constraints and Unreliability - *Lakeshore* Session Chairs Jing-Jia Liou, National Tsing Hua University, Taiwan (Chair) Wujie Wen, Florida International University, USA (Co-Chair) 1) Analysis of Single Event Upsets in Combinational Designs at RTL Based on Satisfiability Modulo Theories, Ghaith Kazma, Ghaith Bany Hamad, Otmane Ait Mohamed and Yvon Savaria 2) Fine-Grain Program Snippets Generator for Mobile Core Design, Shuang Song, Raj Desikan, Mohamad Barakat, Sridhar Sundaram, Andreas Gerstlauer and Lizy K. John 3) Coupling-Aware Functional Timing Analysis for Tighter Bounds: How Much Margin Can We Relax?, Jack S.-Y. Lin, Louis Y.-Z. Lin, Ryan H.-M. Huang and Charles H.-P. Wen 4) Thermal Constrained Energy Efficient Real-Time Scheduling on Multi-Core Platforms, Shi Sha, Wujie Wen, Shaolei Ren and Gang Quan 5) 5) Quantitative Modeling of Thermo-Optic Effects in Optical Networks-on-Chip, Weichen Liu, Peng Wang, Mengquan Li, Yiyuan Xie and Nan Guan	**Session 10:** Memory Design from Circuits to Architectures - *Beehive* Session Chairs Ioannis Savidis, Drexel University, USA (Chair) Selcuk Kose, University of South Florida, USA (Co-Chair) 1) A Reconfigurable Replica Bitline to Determine Optimum SRAM Sense Amplifier Set Time, Samira Ataei and James Stine 2) Building a Fast and Power Efficient Inductive Charge Pump System for 3D Stacked Phase Change Memories, Lei Jiang, Sparsh Mittal and Wujie Wen 3) Design Space Exploration of TAGE Branch Predictor with Ultra-Small RAM, Chaobing Zhou, Libo Huang, Zhisheng Li, Tan Zhang and Qiang Dou 4) A Power Efficient Architecture with Optimized Parallel Memory Accessing for Feature Generation, Peng Ouyang, Shouyi Yin, Chunxiao Xing, Leibo Liu and Shaojun Wei 5) Design of Approximate High-Radix Dividers by Inexact Binary Signed-Digit Addition, Fabrizio Lombardi, Linbin Chen, Weiqiang Liu, Jie Han and Paolo Montuschi	**MS Technical Session 2:** *Plain of Six Glaciers* Moderator: Mohammed Moshirpour, University of Calgary 1) Indiana Bicentennial Torch Project: Trial by Fire, *Todd Wild, Gabriel Martini, Noah Chesnut and Mark Johnson* 2) Teaching Assembly Programming for ARM-based Microcontrollers in a Professional Development Kit, *Weiying Zhu* 3) From Microelectronics to Making: Incorporating Microelectronics in a First-Year Introduction to Engineering Course, *John Nestor* 4) Integrating Emerging Memory Technologies into Undergraduate Logic Design Course: The Impact of Context Based Teaching, *Arifa Hoque, William Sutton, Kawsher Roxy and Sanjukta Bhanja* 5) SF3: A Scalabe and Flexible FPGA-Framework for Education and Rapid Prototyping, *Jan Dürre and Holger Blume*

12:00 – 1:30	**Lunch and Poster Session 2 -** *MT Temple A* Testing/Reliability/Fault-Tolerance, Biochips and Biological Systems, Emerging Computing & Post-CMOS Technologies, Hardware Security Moderator: *Mark Johnson* 1) Throughput Optimization for Lifetime Budgeting in Many Core Systems, Liang Wang, Xiaohang Wang, Ho-Fung Leung and Terrence Mak 2) A Test Pattern Quality Metric for Diagnosis of Multiple Stuck-at and Transition faults, Sarmad Tanwir, Michael Hsiao and Loganathan Lingappan 3) Switched Capacitor and Infinite Impulse Response Summation For A Quarter-Rate DFE With 4Gb/s Data Rate, Gyunam Jeon and Yong-Bin Kim 4) Reducing Microfluidic Very Large Scale Integration (mVLSI) Chip Area by Seam Carving, Brian Crites, Karen Kong and Philip Brisk 5) LUTOSAP: Lookup-Table-Based Online Sample Preparation in Microfluidic Biochips, Lingxuan Shao, Yibin Yang, Hailong Yao and Tsung-Yi Ho 6) ProACt: A Processor for High Performance On-demand Approximate Computing, Arun Chandrasekharan, Daniel Grobe, and Rolf Drechsler 7) Softmax Regression Design for Stochastic Computing Based Deep Convolutional Neural Networks, Zihao Yuan, Ji Li, Zhe Li, Caiwen Ding, Ao Ren, Bo Yuan, Qinru Qiu, Jeffrey Draper and Yanzhi Wang 8) Computing Polynomials with Positive Coefficients using Stochastic Logic by Double-NAND Expansion, Sayed Ahmad Salehi, Yin Liu, Marc Riedel and Keshab Parhi 9) On the Role of Sequential Circuits in Stochastic Computing, Pai-Shun Ting and John Hayes 10) Circuit Techniques for Online Learning of Memristive Synapses in CMOS-Memristor Neuromorphic Systems, Sagarvarma Sayyaparaju, Gangotree Chakma, Sherif Amer and Garrett S. Rose 11) Mitigating Control Flow Attacks in Embedded Systems with Novel Built-in Secure Register Bank, Sean Kramer, Zhiming Zhang, Jaya Dofe and Qiaoyan Yu 12) Using Security Invariant to Verify Confidentiality in Hardware Design, Shuyu Kong, Yuanqi Shen and Hai Zhou 13) Leveraging All-Spin Logic to Improve Hardware Security, Qutaiba Alasad, Jiann Yuan and Deliang Fan **Poster Session MSE:** 1) CloudV: A Cloud-Based Educational Digital Design Environment, Mohamed Shalan and Sherief Reda 2) Work in Progress: MicroElectronics Cloud Alliance. The design of new Open Educational Resources for an Educational Cloud, Rosario Gil-Ortego, Manuel Castro-Gil, Slavka Tzanova and Etienne Sicard 3) WIP: Optimization Algorithms: A Key Component of EDA Education, Florin Balasa and Safaa Mohamed 4) Using Babbage's Difference Engine to Introduce Computer Architecture, William Richard 5) On-die Thermal Evaluation System, Suresh Parameswaran and Boon Ang 6) An Adaptive Senior Design Course with an Emphasis on Undergraduate Course Curriculum, Vishwa Teja Alaparthy and Selcuk Kose

1:30 – 2:50	**Special Session 4:** Efficient IoT Systems: The Power of Heterogeneous Integration - *Lakeshore* Selcuk Kose, University of South Florida (Chair) Ioannis Savidis, Drexel University (Co-Chair) 1) Efficient and Secure On-Chip Reconfigurable Power Delivery for IoT Devices, *Selcuk Kose* 2) Design Space Modeling and Simulation for Physically Constrained 3D CPUs, *Caleb Serafy, Zhiyuan Yang and Ankur Srivastava* 3) Automated Design of Stable Power Delivery Systems for Heterogeneous IoT Systems, *Inna Partin-Vaisband* 4) Work Load Scheduling For Multi Core Systems With Under-Provisioned Power Delivery, *Divya Pathak, Houman Homayoun and Ioannis Savidis*	**Session on Innovation I** - Ideation and Entrepreneurship Mindset - *Beehive* Laleh Behjat, University of Calgary (Chair) *Alex Bruton, Professor of Entrepreneurship, University of Calgary* This highly interactive session will challenge your thinking about what it means to be innovative and entrepreneurial, it will inspire action, and it will provide you with a suite of highly practical tools you can take back to your desk on Monday to lead change at the next whiteboard or on the back of the next napkin you run into.	**Session on Innovation II** - Fostering the Entrepreneurial Mindset Using the KEEN Foundation 3Cs - *Plain of Six Glaciers* *Tina Hudson, Rose-Hulman Institute of Technology* The KEEN foundation believes that every engineer, regardless of position, can benefit from an entrepreneurial mindset. In this interactive workshop, we will describe entrepreneurial mindset learning, the KEEN Foundation's framework for helping every student develop an entrepreneurial mindset, and methods that help you encourage this mindset in your classroom.
2:50 – 3:20	**Coffee Break –** Heritage Hall		
3:20 – 5:30	**Innovation Challenge** - *MT Temple A* Embedded Systems IoT Application Tina Hudson, Rose-Hulman University, USA (Chair) Laleh Behjat, University of Calgary, Canada (Co-Chair) In the Innovation Challenge, you will get to use your Curiosity to experiment in small teams with several sensors on a Cypress Embedded Systems board, and then Integrate this knowledge to propose an application using these sensors. You will defend the Value of your application and the Feasibility of implementation. Each group will present their proposal at the end of the session. Best proposals will win a Cypress board to take home with them.		