Day 1 – Thursday, May 3rd

Keynote Addess 1 – Professor Al Davis, University of Utah (8:30 – 9:30)

- Title: The Role of Photonics in Future Data Centers

Session 1 – Emerging Technologies (10:00 – 12:00): Chaired By: TBD

- "Ambipolar Double-gate FETs for the Design of Compact Logic Structures", Kotb Jabeur, Ian O'Connor, Nataliya Yakymets and Sébastien Le Beux (long)
- "Performance and Energy Models for Memristor-based 1T1R RRAM Cell", Mahmoud Zangeneh and Ajay Joshi (long)
- "Accelerating Thermal Simulations of 3D ICs with Liquid Cooling using Neural Networks", Alessandro Vincenzi, Arvind Sridhar, Martino Ruggiero and David Atienza (long)
- "Efficient CMOL Nanoscale Hybrid Circuit Cell Assignment Using Simulated Evolution Heuristic", Sadiq M. Sait and Abdalrahman M. Arafeh (short)

Session 2 – Reliability (10:00 – 12:00): Chaired By: TBD

- "SNR Analysis Approach for Hardware/Software Partitioning using Dynamically Adaptable Fixed Point Representation", Varadaraj Kamath Nileshwar and Roman Lysecky (long)
- "NBTI Mitigation in Microprocessor Designs", Simone Corbetta and William Fornaciari (long)
- "A Noise-immune Sub-threshold Circuit Design based on Selective Use of Schmitt-trigger Logic", Marco Donato, Fabio Cremona, Warren Jin, R. Iris Bahar, William Patterson, Alexander Zaslavsky and Joseph Mundy (long)
- "Efficient Selection and Analysis of Critical-Reliability Paths and Gates", Jifeng Chen, Shuo Wang and Mohammad Tehranipoor (short)

Poster Session 1 (13:30-14:30)

- "Breaking the Power Delivery Wall using Voltage Stacking", Kaushik Mazumdar and Mircea Stan
- "An Efficient CPI Stack Counter Architecture for Superscalar Processors", Osman Allam, Stijn Eyerman and Lieven Eeckhout

- "An Optimized Multicore Cache Coherence Design for Exploiting Communication Locality", Libo Huang, Zhiying Wang and Nong Xiao
- "Parallel Pipelined FFT Architectures with Reduced Number of Delays", Manohar Ayinala and Keshab Parhi
- "Design of an RNS Reverse Converter for a New Five-Moduli Special Set", Piotr Patronik, Krzysztof Berezowski, Janusz Biernat, Stanislaw Piestrak and Aviral Shrivastava
- "On the Automatic Synthesis of Parallel SW from RTL Models of Hardware IPs", Andrea Acquaviva, Nicola Bombieri, Franco Fummi and Sara Vinco
- "Top-Down-Based Symmetrical Buffered Clock Routing", Jin-Tai Yan, Ming-Chien Huang and Zhi-Wei Chen
- "Optimal Register-Type Selection during Resource Binding in Flip-Flop/Latch-Based High-Level Synthesis", Keisuke Inoue and Mineo Kaneko
- "A Fully Integrated Switched-Capacitor DC-DC Converter with Dual Output for Low Power Application", Heungjun Jeon and Yong-Bin Kim
- "High-level Modeling of Power Consumption in Active Linear Analog Circuits", Laurent Bousquet and Emmanuel Simeu
- "A Novel Power-Gating Scheme Utilizing Data Retentiveness on Caches", Kyundong Kim, Seidai Takeda, Shinobu Miwa and Hiroshi Nakamura
- "A Zero-Overhead IC Identification Technique Using Clock Sweeping and Path Delay Analysis", Nicholas Tuzzio, Kan Xiao, Xuehui Zhang and Mohammad Tehranipoor
- "RAPA: Reliability-Aware Priority Arbitration strategy for Network on Chip", Jiajia Jiao and Yuzhuo Fu
- "A High-Performance Online Assay Interpreter for Digital Microfluidic Biochips", Daniel Grissom and Philip Brisk
- "Reliable Logic Mapping on Nano-PLA Architectures", Masoud Zamani and Mehdi Tahoori

Session 3 – Circuit Design (14:30 – 16:10): Chaired by TBD

- "Self Adaptive Body Biasing Scheme For Leakage Power Reduction In Nanoscale CMOS Circuit", Jing Yang and Yong-Bin Kim (long)
- "Synchronization Scheme for Brick-based Rotary Oscillator Arrays", Ying Teng and Baris Taskin (long)
- "A Low-Power All-Digital GFSK Demodulator with Robust Clock Data Recovery", Pengpeng Chen, Bo Zhao, Rong Luo and Huazhong Yang (short)
- "Link Breaking Methodology: Mitigating Noise within Power Networks", Renatas Jakushokas and

Eby G. Friedman (short)

Session 4 – CAD-I (14:30 – 16:10): Chaired By: TBD

- "Unifying Functional and Parametric Timing Verification", Luis Guerra E Silva (long)
- "New & Improved Models for SAT-Based Bi-Decomposition", Huan Chen and Joao Marques-Silva (long)
- "Lithography-Aware Layout Compaction", Curtis Andrus and Matthew Guthaus (short)
- "A Design Approach Dedicated to Network-Based and Conflict-Free Parallel Interleavers", Aroua Briki, Cyrille Chavet, Philippe Coussy and Eric Martin (short)

Session 5 – Multi-core and NOC (16:30 – 18:10): Chaired By: TBD

- "Distributed Sensor Data Processing for Many-cores", Jia Zhao, Russell Tessier and Wayne Burleson (long)
- "CMOS Compatible Many-Core NoC Architectures with Multi-Channel Millimeter-Wave Wireless Links", Sujay Deb, Kevin Chang, Miralem Cosic, Amlan Ganguly, Partha Pande, Deukhyoun Heo and Benjamin Belzer (long)
- "Voltage Island-Driven Power Optimization For Application Specific Network-on-Chip Design", Kan Wang, Sheqin Dong and Satoshi Goto (short)
- "Design-Time Performance Evaluation of Thermal Management Policies for SRAM and RRAM based 3D MPSoCs", David Brenner, Cory Merkel and Dhireesha Kudithipudi (short)

Session 6 – Testing and Fault-Tolerance (16:30 – 18:10): Chaired By: TBD

- "TSUNAMI: A Light-Weight On-Chip Structure for Measuring Timing Uncertainty Induced by Noise During Functional and Test Operations", Shuo Wang and Mohammad Tehranipoor (long)
- "Lazy Suspect-Set Computation: Fault Diagnosis for Deep Electrical Bugs", Dipanjan Sengupta, Flavio M. De Paula, Alan J. Hu, Andreas Veneris and André Ivanov (long)
- "Influence of Different Layout Styles on the Performance of the Calibration of an On-Chip Programmable Voltage Reference", Dominik Gruber and Timm Ostermann (short)
- "Input and Transistor Reordering for NBTI and HCI Reduction in Complex CMOS Gates", Saman Kiamehr, Farshad Firouzi and Mehdi B. Tahoori (short)

Day 2 – Friday, May 4th

Keynote Addess 2 – Professor Khaled Salama, King Abdullah University of Science and Technology (8:30 – 9:30)

- Title: "Memristor: The Illusive Device"

Session 7 – Post-CMOS Circuits (10:00 – 12:00): Chaired By: TBD

- "InMnAs Magnetoresistive Spin-Diode Logic", Joseph S. Friedman, Nikhil Rangaraju, Yehea I. Ismail and Bruce W. Wessels. (long)
- "An Efficient Approach for Designing and Minimizing Reversible Programmable Logic Arrays", Sajib Kumar Mitra, Lafifa Jamal, Mineo Kaneko, and Hafiz Md. Hasan Babu. (long)
- "Modeling a Single Electron Turnstile in HSPICE", Fabrizio Lombardi, Wei Wei, and Jie Han (long)
- "Limits of Writing Multivalued Resistances in Passive Nanoelectronic Crossbars Used in Neuromorphic Circuits", Arne Heittmann and Tobias G. Noll (short)

Session 8 – Low Power (10:00 – 12:00): Chaired By: TBD

- "Stepwise Sleep Depth Control for Run-Time Leakage Power Saving", Seidai Takeda, Shinobu Miwa, Kimiyoshi Usami and Hiroshi Nakamura (long)
- "An Efficient Power Estimation Methodology for Complex RISC Processor-based Platforms", Santhosh Kumar Rethinagiri, Rabie Ben Atitallah, Jean-Luc Dekeyser, Eric Senn and Smail Niar (long)
- "ADAM: An Efficient Data Management Mechanism for Hybrid High and Ultra-Low Voltage Operation Caches", Bojan Maric, Jaume Abella and Mateo Valero (long)
- "A Low Stand-by Power Start-up Circuit for SMPS PWM Controller", In-Seok Jung and Yong-Bin Kim (short)

Poster Session 2 (13:30-14:30)

- "Particle Swarm Optimization over Non-Polynomial Metamodels for Fast Process Variation Resilient Design of Nano-CMOS PLL", Oleg Garitselov, Saraju Mohanty, Elias Kougianos and Geng Zheng
- "A Denial-of-Service Resilient Wireless NoC Architecture", Amlan Ganguly, Mohsin Yusuf Ahmed and

Anuroop Vidapalapati

- "Sustainable Multi-Core Architecture with on-chip Wireless Links", Jacob Murray, John Klingner, Partha Pande and Behrooz Shirazi
- "SRAM Leakage in CMOS, FinFET and CNTFET Technologies", Zhe Zhang, Michael A. Turi and Jose G. Delgado-Frias
- "A Novel Hybrid FIFO Asynchronous Clock Domain Crossing Interfacing Method", Zaid Al-Bayati, Otmane Ait Mohamed, Syed Rafay Hasan, and Yvon Savaria
- "Density-Reduction-Oriented Layer Assignment for Rectangle Escape Routing", Jin-Tai Yan, Jun-Min Chung and Zhi-Wei Chen
- "NBTI Effects on Tree-Like Clock Distribution Networks", Wei Liu, Sandeep Miryala, Valerio Tenace, Andrea Calimera, Enrico Macii and Massimo Poncino
- "A Framework for High-Level Synthesis of Heterogeneous MP-SoC", Youenn Corre, Jean-Philippe Diguet, Dominique Heller and Loïc Lagadec
- "Memory-based Computing for Performance and Energy Improvement in Multicore Architectures", Kamran Rahmani, Prabhat Mishra and Swarup Bhunia
- "Share Memory Aware Scheduler: Balancing Performance and Fairness", Xi Li, Gangyong Jia, Yun Chen, Zongwei Zhu, and Xuehai Zhou
- "Alleviating NBTI-induced Failure in Off-chip Output Drivers", Bhavitavya Bhadviya, Ayan Mandal and Sunil Khatri
- "Mitigating Electromigration of Power Supply Networks Using Bidirectional Current Stress", Jing Xie, Vijaykrishnan Narayanan and Yuan Xie
- "Multiplexed Switch Box Architecture in Three-dimensional FPGAs to Reduce Silicon Area and Improve TSV Usage", Marzieh Morshedzadeh and Ali Jahanian
- "A Scalable Threshold Logic Synthesis Method Using ZBDDs", Ashok Kumar Palaniswamy and Spyros Tragoudas
- "A Memristor-based TCAM (Ternary Content Addressable Memory) Cell: Design and Evaluation", Pilin Junsangsri and Fabrizio Lombardi

Session 9 – CAD-II (14:30 – 16:10): Chaired By: TBD

- "Extending Symmetric Variable-Pair Transitivities Using State-Space Transformations", Peter M. Maurer (long)
- "Crosslink Insertion for Variation-Driven Clock Network Construction", Fuqiang Qian, Haitong Tian and Evangeline Young (long)
- "WRIP: Logic Restructuring Techniques for Wirelength-Driven Incremental Placement", Xing

Wei, Wai-Chung Tang, Yu-Liang Wu, Cliff Sze and Charles Alpert (short)

- "STEP: A Unified Design Methodology for Secure Test and IP Core Protection", Pranav Yeolekar, Rishad A. Shafik, Jimson Mathew, Dhiraj K. Pradhan, and Saraju Mohanty (short)

Session 10 – VLSI Systems (14:30 – 16:10): Chaired By: TBD

- "Towards Systolic Hardware Acceleration for Local Complexity Analysis of Massive Genomic Data", Agathoklis Papadopoulos, Vasilis Promponas and Theocharis Theocharides (long)
- "A Dual-Phase Compression Mechanism for Hybrid DRAM/PCM Main Memory Architectures", Seungcheol Baek, Hyung Gyu Lee, Chrysostomos Nicopoulos and Jongman Kim (short)
- "Verilog-AMS-PAM: Verilog-AMS integrated with Parasitic-Aware Metamodels for Ultra-Fast and Layout-Accurate Mixed-Signal Design Exploration", Geng Zheng, Saraju Mohanty, Elias Kougianos and Oleg Garitselov (short)
- "Efficient Folded VLSI Architectures for Linear Prediction Error Filters", Sayed Ahmad Salehi, Rasoul Amirfattahi and Keshab Parhi (short)
- "Synergistic Integration of Code Encryption and Compression in Embedded Systems", Kamran Rahmani, Hadi Hajimiri, Kartik Shrivastava and Prabhat Mishra (short)