Day 1 - Monday, May 2nd

Keynote Addess 1 – Prof. Rajesh Gupta UCSD, USA (8:30 – 9:30)

- "Sensing and Sensibility of Energy Use in Modern Mixed-Use Buildings"

Session 1 – Emerging Technologies (10:00 – 12:00): Chaired by Mircea Stan

- "An Arbiter Based On-chip Droop Detector System", Jinwook Jang and Wayne Burleson
- "A Programmable and Scalable Technique To Design Spintronic Logic Circuits Based On Magnetic Tunnel Junctions", Shruti Patil and David Lilja
- "Logic Synthesis for Integrated Optics", Christopher Condrat, Priyank Kalla and Steve Blair
- "Fine-Grain Reconfigurable Logic Cells Based on Double-gate CNTFETs", kotb jabeur, natalya yakymets, Ian O'Connor and Sébastien Le-Beux
- "A Self-Assembled Multiferroic Magnetic QCA for Low Power Systems", Mehdi Kabir, Mircea Stan and Stuart Wolf

Special Session 1 - SMECY : programming tool chains for multi-core platforms (10:00 – 12:00): Chaired By: Donatella Sciuto

Poster Session 1 (13:15-14:15)

- "Design and Failure Analysis of Logic-Compatible Multilevel Gain-Cell-Based DRAM for Fault-Tolerant VLSI Systems", Pascal Meinerzhagen, Onur Andic, Jurg Treichler and Andreas Burg
- "Power Efficient Partial Product Compression", Chiu-wei Pan, Zhao Wang, Yuanchen Song and Carl Sechen
- "Evaluation of FPGA Routing Architectures Under Process Variation", Fatemeh Poorhashemi and Morteza Saheb Zamani
- "High Resolution MASH 2-2 Sigma-Delta Interface for Capacitive Accelerometers", swathi ramasahayam and Satyam Mandavilli
- "Influence of Metallic Tubes on the Reliability of CNTFET SRAMs: Error Mechanisms and Countermeasures", Zhen Wang, Ajay Joshi and Mark karpovsky
- "A new Low Power and area efficient semi-digital PLL architecture for low bandwidth applications", Puneet Sareen and Markus Dietl
- "SIAR: Splitting-Graph-Based Interactive Analog Router", Fan Yang, Hailong Yao, Qiang Zhou and Yici Cai

- "A Comparative Study of State-of-The-Art Low-Power CAM Match-Line Sense Amplifier Designs", Anh Tuan Do, Xiao Liang Tan, Shou Shun Chen, Zhi Hui Kong and Kiat Seng Yeo
- "Sensitivity of Neuromorphic Circuits Using Nanoelectronic Resistive Switches to Pulse Synchronization", Arne Heittmann and Tobias G. Noll
- "A Dual-Core System Solution for Wearable Health Monitors", Frank Bouwens, Jos Huisken, Harmke De Groot, Martijn Bennebroek, Anteneh Abbo, Octavio Santana, Jef van Meerbergen and Antoine Fraboulet

Day 2 - Tuesday, May 3rd

Keynote Addess 2 – Dr. Sani R. Nasif IBM, USA (7:30 – 8:30)

- "Waiting for the Post-CMOS Godot"

Session 2 - NoCs and Routing (8:30-10:30): Chaired By: Martino Ruggiero

- "VISION: A Framework for Voltage Island Aware Synthesis of Interconnection Networks-on-Chip", Nishit Kapadia and Sudeep Pasricha
- "Rover: Routing on Via-Configurable Fabrics for Standard-Cell-Like Structured ASICs", Liang-Chi Lai, Hsih-Hang Chang and Rung-Bin Lin
- "Run-Time Energy Management of Manycore Systems Through Reconfigurable Interconnects", Jie Meng, Chao Chen, Ayse Coskun and Ajay Joshi
- "Congestion and Track Usage Improvement of Large FPGAs Using Metro-on-FPGA Methodology", Mehdi Alipour, Mohammad Haji Seyed Javadi and Ali Jahanian
- "Multi-objective Topology Synthesis and FPGA Prototyping Framework of Application Specific Network-on-Chip", Xinyu LI and Omar Hammami

Special Session 2 - Magnetic memory (MRAM) A New Area for 2D and 3D SoC/SiP Design (8:30-10:30): Chaired By: Lionel Torres

Session 3 - Circuit Design I (11:00-13:00): Chaired By: Andreas Burg

- "Efficient Shift-Adds Design of Digit-Serial Multiple Constant Multiplications", Levent Aksoy, Cristiano Lazzari, Eduardo Costa, Paulo Flores and Jose Monteiro
- "Accelerating Itoh-Tsujii Multiplicative Inversion Algorithm for FPGAs", Sujoy Sinha Roy, Chester Rebeiro and Debdeep Mukhopadhyay
- "FPGA implementation of Binary Edwards Curve using ternary representation", Ayantika Chatterjee and

Indranil Sengupta

- “Design of Low-Power Multiple Constant Multiplications Using Low-Complexity Minimum Depth Operations”, Levent Aksoy, Eduardo Costa, Paulo Flores and Jose Monteiro
- "High Performance Technique for Database Applications Using a Hybrid GPU/CPU Platform”, M. Affan Zidan, Talal Bonny and Khaled N. Salama
- “Design and Management of 3D-Stacked NUCA Cache for Chip Multiprocessors”, Jongpil Jung, Kyungsu Kang and Chong-Min Kyung

Special Session 3 - Quantum Devices and Optical Computing: Chaired By: Braulio Garcia-Camara

Session 4 - Low Power and Temperature (14:00-16:00): Chaired By: Kivilcim Coskun

- “DRAM Energy Reduction by Prefetching-Based Memory Traffic Clustering”, Yebin Lee and Soontae Kim
- “A Low-Power TCAM Design Using Mask-Aware Match-Line (MAML) Technique”, Yen-Jen Chang and Tung-Chi Wu
- “Hardware-assisted Dynamic Power and Thermal Management in Multi-core SoCs”, George Kornaros
- "A 7T SRAM Bit-cell for Low-Power Embedded Memories”, Wasim Hussain and Shah M. Jahinuzzaman

Special Session 4 - Hardware Security in VLSI (14:00-16:00): Chaired By: Wayne Burleson

Poster Session 2 (16:00-17:00)

- “Robust Signaling Techniques for Through Silicon Via Bundles”, Krishna Chillara, Jinwook Jang and Wayne Burleson
- “Efficient Realization of RTD-CMOS Logic Gates”, Juan Núñez, María J. Avedillo and José M. Quintana
- “On Residue Removal in Digital Microfluidic Biochips”, Debasis Mitra, Sarmishtha Ghoshal, Hafizur Rahaman, Krishnendu Chakrabarty andBhargab B. Bhattacharya
- “Repeater Insertion in Power-Managed VLSI Systems”, Houman Zarrabi, Asim Al-Khalili and Yvon Savaria
- “Experimental Demonstration of Standby Power Reduction using Voltage Stacking in an 8Kb Embedded FDSOI SRAM”, Adam Cabe and Mircea Stan
- “Handling Intra-Die Variations in PSTA”, Luis Guerra e Silva and L. Miguel Silveira
- “Integrated Logic Synthesis Using Simulated Annealing”, Petra Färm, Elena Dubrova and Andreas Kuehlmann
- “A Geometric Programming Aided Knowledge based Approach for Analog Circuit Synthesis and Sizing”,

Supriyo Maji and Pradip Mandal

- "Analyzing Throughput of Power and Thermal-constraint Multicore Processor under NBTI Effect", Shi-Qun Zheng, Ing-Chao Lin and Yen-Han Lee
- "Efficient Method to Compute Minimum Decision Chains of Boolean Functions", Mayler Martins, Vinicius Callegaro, Renato Ribas and Andre Reis
- "Time-Mode Reconstruction IIR Filters for ∑Δ Phase Modulation Applications", Ali Ameri and Gordon W. Roberts

Day 3 - Wednesday, May 4th

Session 5 - Circuit Design II (10:30-12:30): Chaired By: Andre Reis

- "A Static-Switching Pulse Domino Technique for Statistical Power Reduction of Wide Fan-in Dynamic Gates", Rahul Singh and Suhwan Kim
- "A 45.6μ^2 13.4μW 7.1V/V Resolution Sub-Threshold Based Digital Process-Sensing Circuit in 45nm CMOS", Basab Datta and Wayne Burleson
- "A New Balanced 4-moduli Set {2^k,2^n-1,2^n+1,2^{n+1}-1} and its Reverse Converter Design for Efficient FIR Filter Implementation", Gayathri Chalivendra, Vinay Hanumaiah and Sarma Vrudhula
- "Towards Robust Nano-CMOS Sense Amplifier Design: A Dual-Threshold versus Dual-Oxide Perspective", Oghenekarho Okobiah, Saraju Mohanty and Elias Kougianos
- "A Design Methodology for the Automatic Sizing of Standard-Cell Libraries", Christian Pilato, Fabrizio Ferrandi and Davide Pandini

Session 6 - Asynchronous circuits (10:30-12:30): Chaired By: Román Hermida

- "Integration of Behavioral Synthesis and Floorplanning for Asynchronous Circuits with Bundled-data Implementation", Naohiro Hamada and Hiroshi Saito
- "Coupling Latency-Insensitivity with Variable-Latency for Better Than Worst Case Design: A RISC Case Study", Mario R. Casu, Stefano Colazzo and Paolo Mantovani
- "Technology Mapping for Power using Threshold Logic Cells", Niranjan Kulkarni and Sarma Vrudhula
- "Reconfigurable Controllers for Synchronization via Wagging", James Guido and Alexandre Yakovlev
- "Variation-Immune QDI Implementation on Nano-Crossbar Arrays", Masoud Zamani and Mehdi B. Tahoori

Session 7 – CAD (10:30-12:30): Chaired By: Massimo Poncino

- "An Efficient Algorithm for Custom Instruction Enumeration", Chenglong Xiao and Emmanuel Casseau

- “An Approximation Algorithm for Cofactoring-Based Synthesis”, Anna Bernasconi, Valentina Ciriani, Valentino Liberali, Gabriella Trucco and Tiziano Villa
- “Obstacle-avoiding and Slew-constrained Buffered Clock Tree Synthesis for Skew Optimization”, Feifei Niu, Qiang Zhou, Hailong Yao, Yici Cai, Jianlei Yang and Cliff Sze
- “New Optimal Layer Assignment for Bus-Oriented Escape Routing”, Jin-Tai Yan and Zhi-Wei Chen
- “Acceleration of Random-walk-based Linear Circuit Analysis using Importance Sampling”, Tetsuro Miyakawa, Koh Yamanaga, Hiroshi Tsutsui, Hiroyuki Ochi and Takashi Sato

Session 8 - Design of Specific Circuits (14:00-16:00)

- “A 65nm CMOS Low-Power RF Front-End for L1/E1 GPS/Galileo Signals”, Gaetano Rivela, Pietro Scavini, Daniele Grasso, Antonino Calcagno, Maria Gabriella Castro, Giuseppe Di Chiara, Giuseppe Avellone, Giovanno Cali' and Salvatore Scaccianoce
- “Simulation-based Equivalence Checking between SystemC Models at different Levels of Abstraction”, Daniel Grosse, Ulrich Kuehne, Markus Gross and Rolf Drechsler
- “Fast high-performance algorithms for multi-pin droplet routing in Digital Microfluidic Biochips” Pranab Roy, Hafizur Rahaman and Parthasarathi Dasgupta
- “A Countermeasure Against Power Analysis Attacks for FSR-Based Stream Ciphers”, Shohreh Sharif Mansouri and Elena Dubrova
- “Optimal Memory Controller Placement in On-chip Interconnection Networks”, Masoud Dehyadegari, Siamak Mohammadi and Naser Yazdani
- “Low Jitter Audio Range PLL with ultra low Power Dissipation”, Fu Lou and Godi Fischer

Session 9 - Design for variability (14:00-16:00)

- “Layout-aware Variation Evaluation of Analog Circuits and Its Validity on Op-amp Designs”, Kota Shinohara, Mihoko Hidaka, Jing Li, Qing Dong, Bo Yang and Shigetoshi Nakatake
- “A Linear Programming Approach for Minimum NBTI Vector Selection”, Farshad Firouzi, Saman Kiamehr and Mehdi B. Tahoori
- “Fitting Standard Cell Performance to Generalized Lambda Distributions”, André Lange, Haase and Mau
- “Stress Aware Switching Activity Driven Low Power Design of Critical Paths in Nanoscale CMOS Circuits”, SUDARSHAN SRINIVASAN, Bharath Phanibhushana, ARUNKUMAR VIJAYAKUMAR and Sandip Kundu
- “Simultaneous Variation-Aware Architecture Exploration and Task Scheduling for MPSoC Energy Minimization”, Mahmoud Momtazpour, Mahboobeh Ghorbani, Maziar Goudarzi and Esmaeil Sanaei

Session 10 - Design for reliability (16:30-18:30): Chaired By: Mehdi Tahoori

- “Impact of Positive Bias Temperature Instability (PBTI) on 3T1D-DRAM Cells”, Nivard Aymerich, Shrikanth Ganapathy, Antonio Rubio, Ramon Canal and Antonio González
- “Redundancy in SAR ADCs”, Albert H. Chang, Duane Boning and Hae-Seung Lee
- “A High Sensitivity and Process Tolerant Digital Thermal Sensing Scheme for Liquid Cooled 3-D Ics”, Basab Datta and Wayne Burleson
- “Buffering of Frequent Accesses for Reduced Cache Aging”, Andrea Calimera, Mirko Loghi, Enrico Macii and Massimo Poncino
- “Combined Architecture and Hardening Techniques Exploration for Reliable Embedded System Design”, Cristiana Bolchini, Antonio Miele and Christian Pilato
- “Ordered Coloring-Based Resource Binding for Datapaths with Improved Skew-Adjustability”, Mineo Kaneko and Keisuke Inoue

Session 11 - Circuit Design III (16:30-18:30)

- “Power Estimation of Dividers Implemented in FPGAs”, Ruzica Jevtic, Bojan Jovanovic and Carlos Carreras
- “Nanometer-scale Standard Cell Library for Enhanced Redundant Via1 Insertion Rate”, Tsang-Chi Kan, Shih-Hsien Yang, Ting-Feng Chang and Shanq-Jang Ruan
- “Circuit Design of a Dual-Versioning L1 Data Cache for Optimistic Concurrency”, Azam Seyedi, Adrià Armejach, Osman Unsal, Adrián Cristal, Ibrahim Hur and Mateo Valero
- “Real-Time Address Trace Compression for Emulated and Real System-on-Chip Processor Core Debugging”, Bojan Mihajlovic and Zeljko Zilic
- “Investigating Modern Layout Representations for Improved 3D Design Automation”, Robert Fischbach, Jens Lienig and Johann Knechtel