An Integrated Thermal Estimation Framework for Industrial Embedded Platforms

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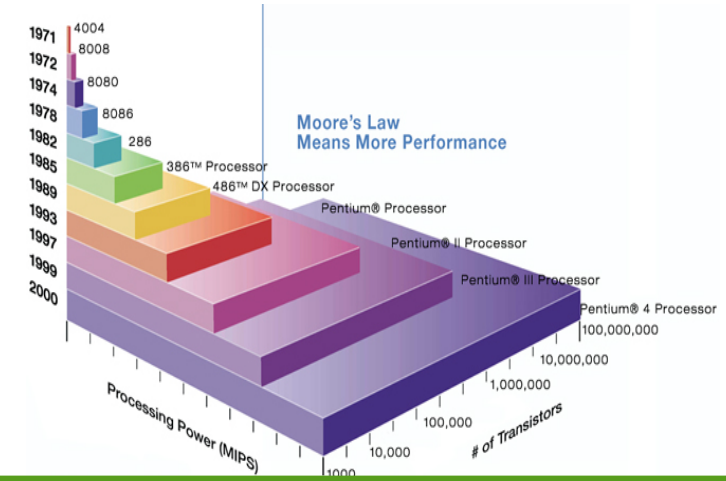
… Because Temperature Matters !

Technology scaling



Intrusive thermal-aware design techniques are required at each level of abstraction

Efficient application of these techniques requires fast thermal estimations at each stage of the design flow

MORE GENERATED HEAT

DIFFICULTIES IN DISSIPATING HEAT

THERMAL ISSUES

- High Operating Temperature
- Large Temperature Gradient

CIRCUIT PERFORMANCE

RELIABILITY and AGING

POWER CONSUMPTION

Thermal-Aware Design

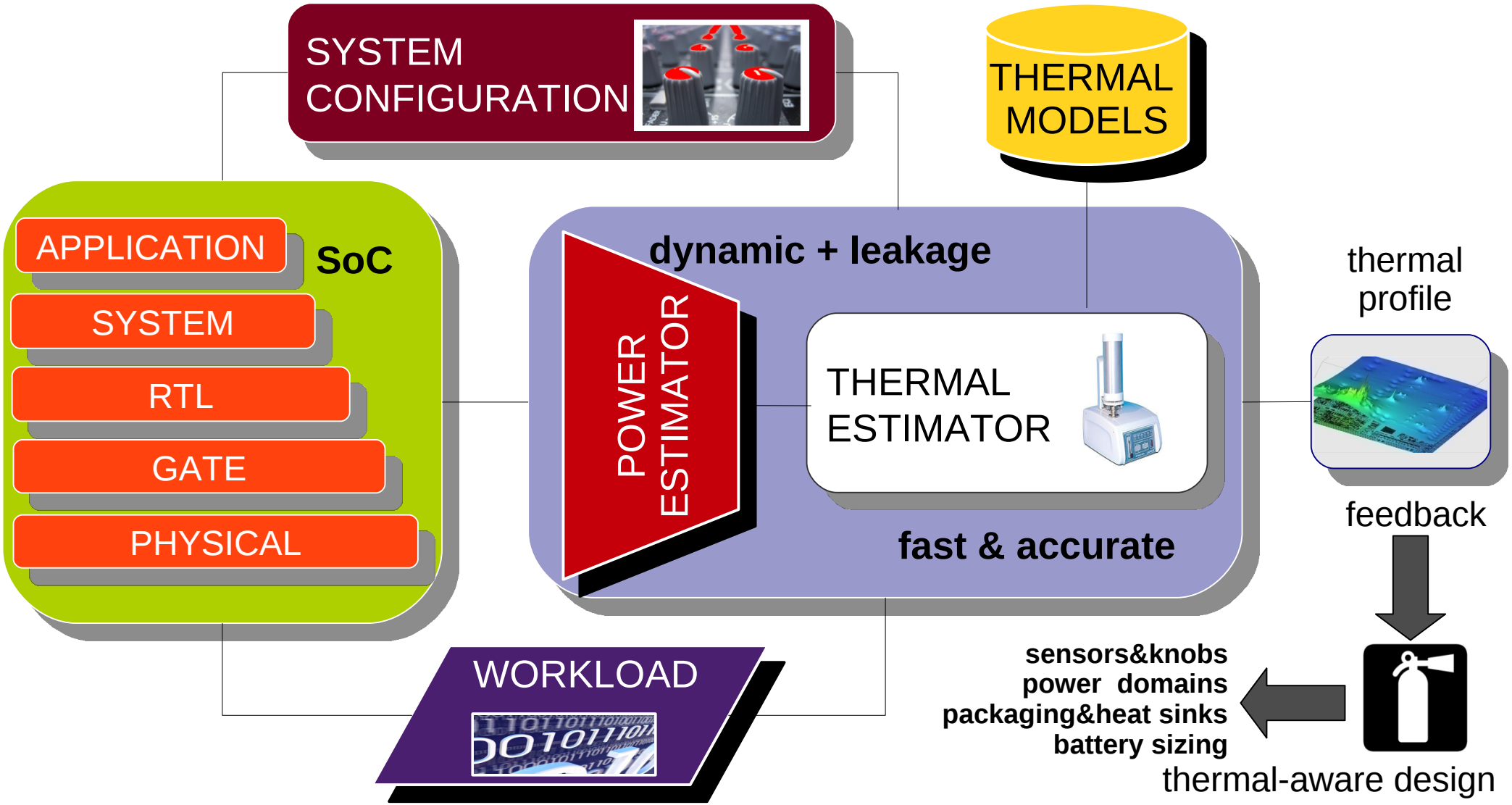
- Intrusive thermal-aware design techniques have become a must in modern SoCs, at each level of abstraction
  - application level (e.g., thermal aware task migration)
  - system level (e.g., 3D ICs, packaging, heat spreading)
  - architectural level (e.g., Measure & Control techniques - DVFS)
    - temperature monitors
    - knobs which implement control strategies
- Efficient application of these strategies requires fast estimation of thermal effects in the earlier stages of the SoC design flows
  - spatial&temporal gradients
  - peak operating temperature and hotspots

A thermal estimation framework which integrates heterogeneous info - at design time - is missing in today's flow

Outline

- An ideal thermal estimator... just alchemy?
- Why it is so hard... an industrial test case
- Power/thermal estimation flow
- What you can do
  - Single component analysis
  - Component interaction analysis
- Conclusions

Heterogeneous Thermal Estimator



ST Spear 1300 MPU: Mean Features

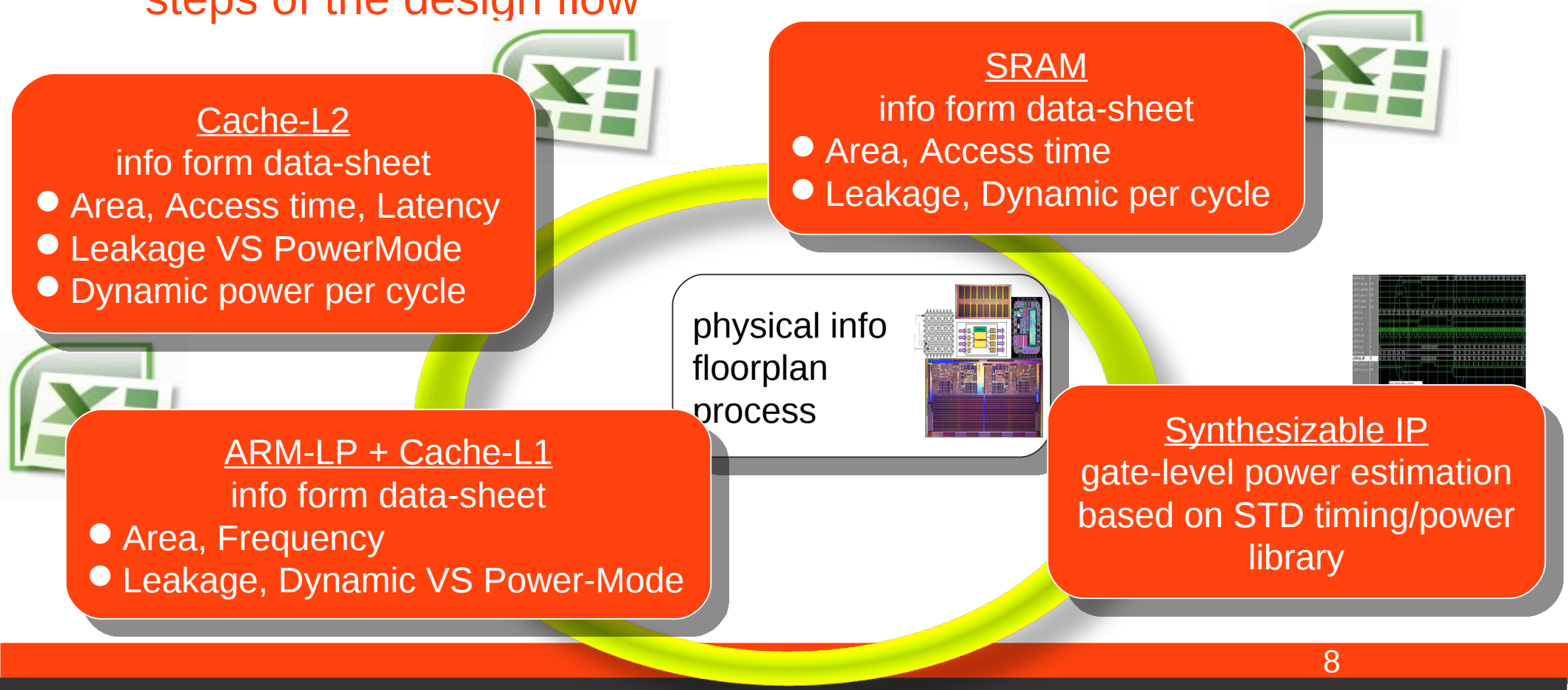
- Designed for cost-sensitive applications requiring significant processing and connectivity capabilities at low power consumption
  - networking/home gateways (eth and WiFi interface)
  - embedded media and imaging (camera interface, LCD/touch screen controller, audio codecs)
- Architecture
  - ARM A9 Cortex dual-core power-optimized 800MHz
  - 512KB L2 Cache
  - Serial Management Interface (SMI - IP)
  - One-time programmable logic (anti-fuse)
  - 300KB SRAM Memory

ST Spear 1300 MPU: Low-Power

- Advanced power savings features
  - Multiple power mode: Normal, Slow, Sleep mode
  - CPU clock with software programmable frequency
  - Multiple power domains
    - Dual-core CPU
    - configurable logic
    - PCI controllers
    - Memories
    - I/O peripheral
  - 2 levels of coarse-grain clock-gating structures for each power domain
  - Power-aware physical synthesis using low-power libraries with dual threshold voltage cell usage

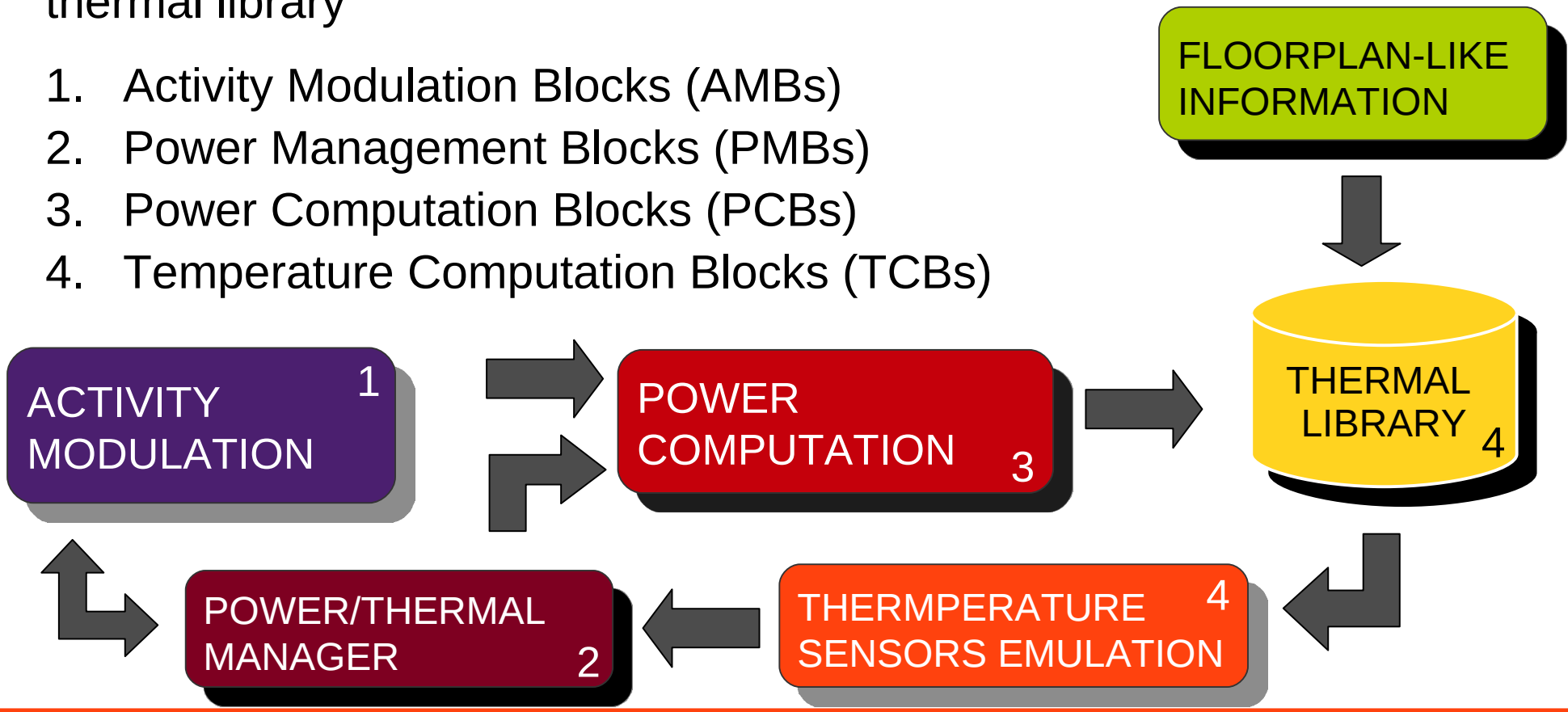
Heterogeneous Power Information

- A smart power estimator should be able to integrate mixed information obtained using different techniques at different steps of the design flow



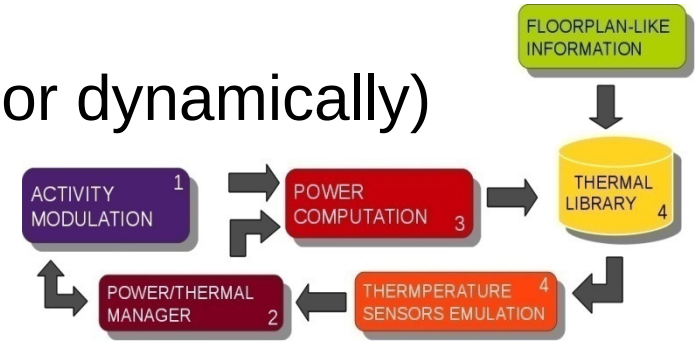
Power/Thermal Estimation Flow

- An unique environment based on Matlab Simulink® which integrates different power estimation techniques and interfaces with a thermal library
  1. Activity Modulation Blocks (AMBs)
  2. Power Management Blocks (PMBs)
  3. Power Computation Blocks (PCBs)
  4. Temperature Computation Blocks (TCBs)



Activity Modulation Blocks (AMBs)

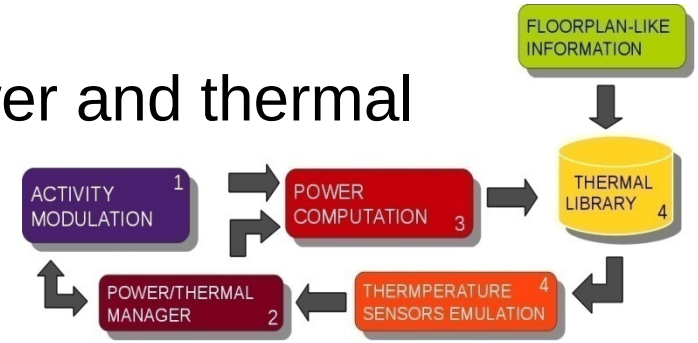
- AMBs set the utilization profiles (statically or dynamically) of the system components
- Implemented using Simulink Stateflow®
  - design environment for state charts and flow diagram
- For each component of the SoC
  - the functionality is described as a finite state machine
  - the activity is defined as states and transitions among theme triggered by self-generated or asynchronous external events



Component	AMBs	Output
IPs	FSM	Switching activity over time
Hard Macro	Power-State Machine	Power-state currently in use
Memory	Memory access emulation of a trace	# read/write operation cycles

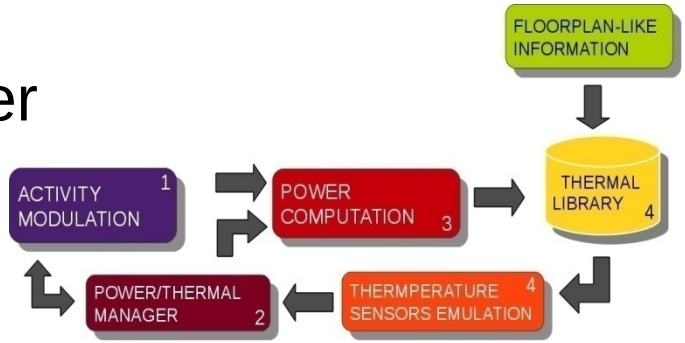
Power Management Blocks (PMBs)

- PMBs simulate the implementation of power and thermal management policies
- Implemented using Matalb Simulink®
- Interact with AMBs, PCBs and TCBs
  - take the activity information from AMBs and the thermal information coming from the thermal feedback
  - decide when to enter a certain power state configuration
  - the power configuration is used inside PCBs to compute actual power consumption
  - e.g., if a component is idle (info from AMBs), it is turned into a power-gating state (by PMBs); this info will be used to calculate the effective power consumption (info to PCBs)



Power Computation Blocks (PCBs)

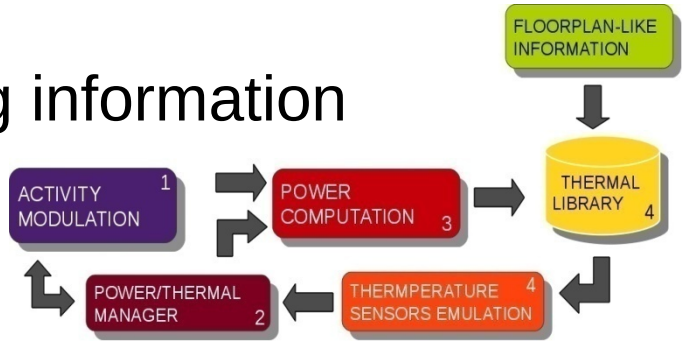
- PCBs compute dynamic and leakage power consumption
- Implemented using different techniques depending on the type of components and the power characterizations available

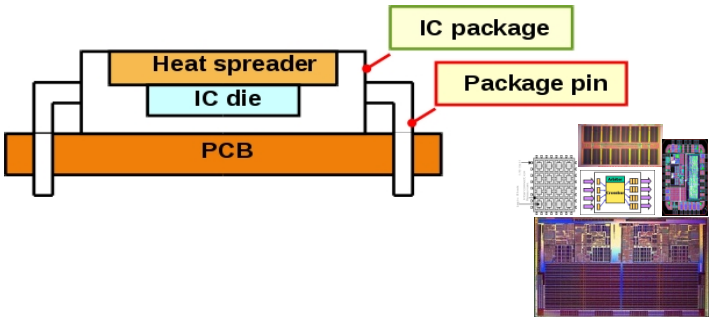


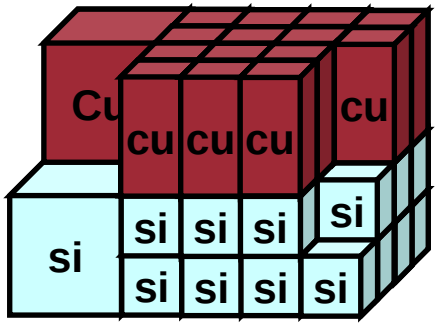
COMPONENT	AVAILABLE INFO	DESCRIPTION
Core processor + L1 cache	Power state information	● It is the only info available for hard macros ● Power consumption quantified for the given tech. and for various corner cases (WC, NOM, BC, temperature) ● Static and available for each power mode
Memories (L2 cache, SRAM)	Energy per read/write cycle	● Total leakage and dynamic power per cycle for various corner cases and operating conditions (Voltage, Temp.)
Synthesizable IPs	Gate-level netlist + switching activity analysis + tech.libs	● Accurate power estimation using standard library characterization provided by silicon vendors ● Statistical analysis is performed by imposing a probabilistic switching activity on the input ports of the IP

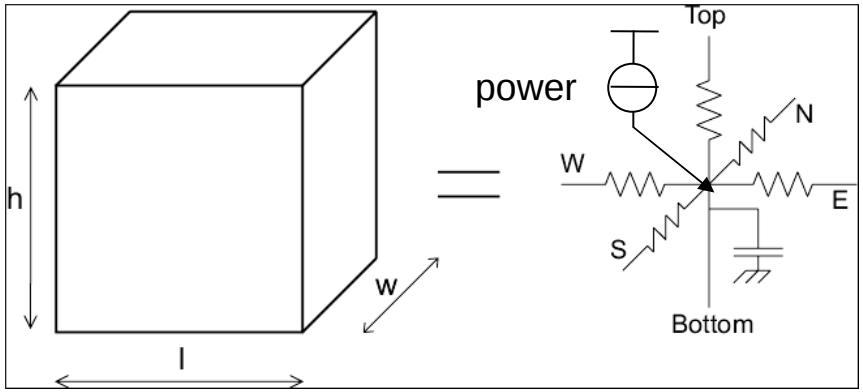
Thermal Computation Blocks (TCBs)

- TCBs provide thermal estimation exploiting information about component area and position
  - power consumption data are sampled at predefined time intervals (speed/accuracy) and converted into power-density
  - data are fitted into the thermal library and an equivalent RC electrical model is generated
  - emulated sensors provide temperature (voltage measurement on the RC model)









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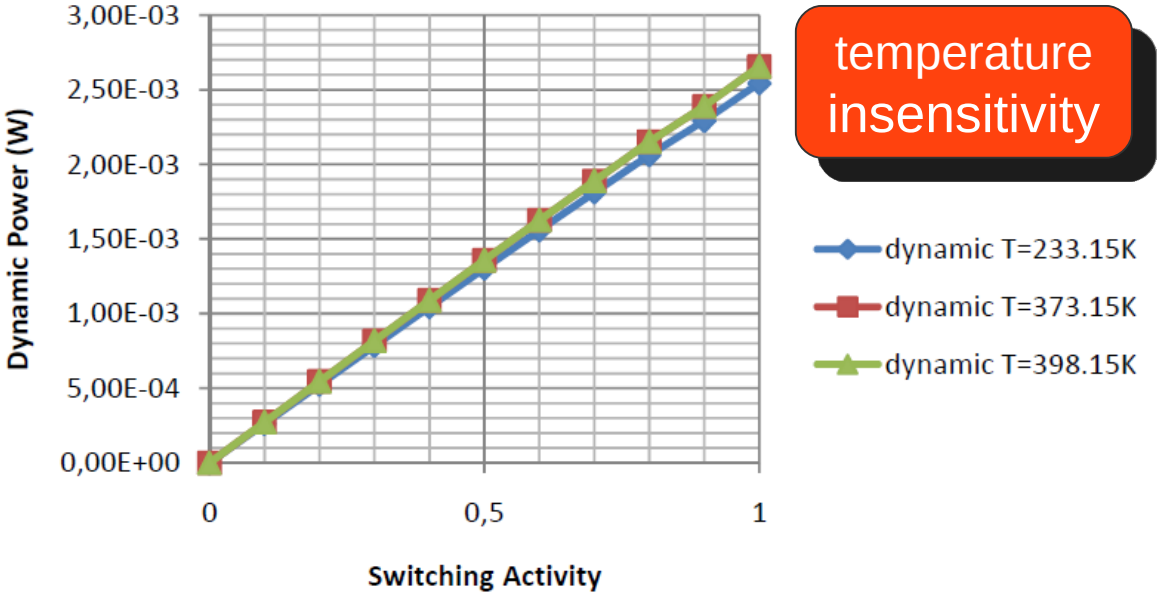
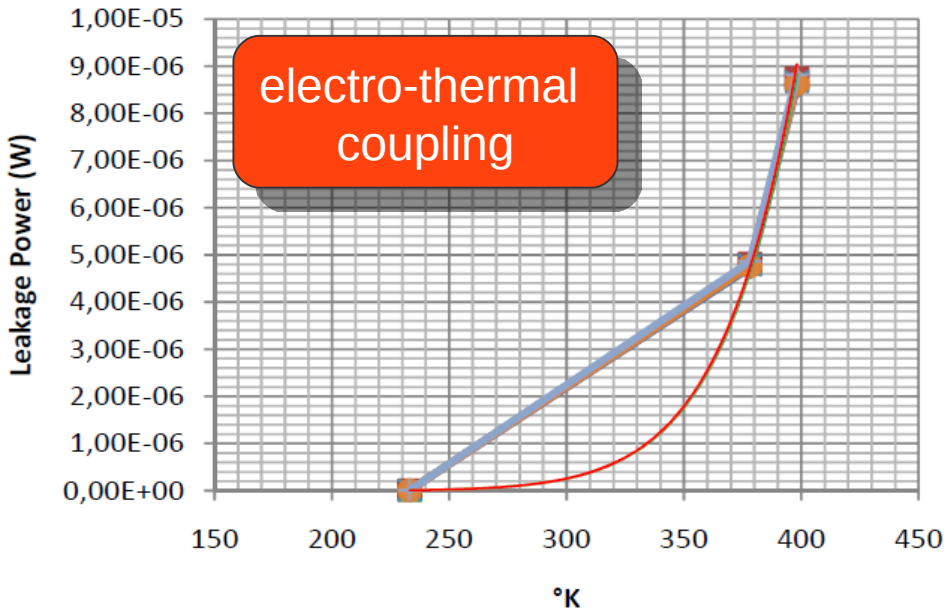
Single Component Analysis

- A component is selected using the component selection mask, while the rest of the chip remains at a given initial temperature
- Used for two purposes
  - simulate a realistic functional behavior for a specific use case or power management configuration
  - evaluate the the self-heating that specific component independently from the surroundings
- Serial Management Interface (SMI)
  - Power oriented dual-Vth synthesis
  - STMicrolectronics 65nm STM tech.
  - Power characterization under different PVT corners

SMI Power Characterization

- Dynamic and Leakage power characterization under different input activity



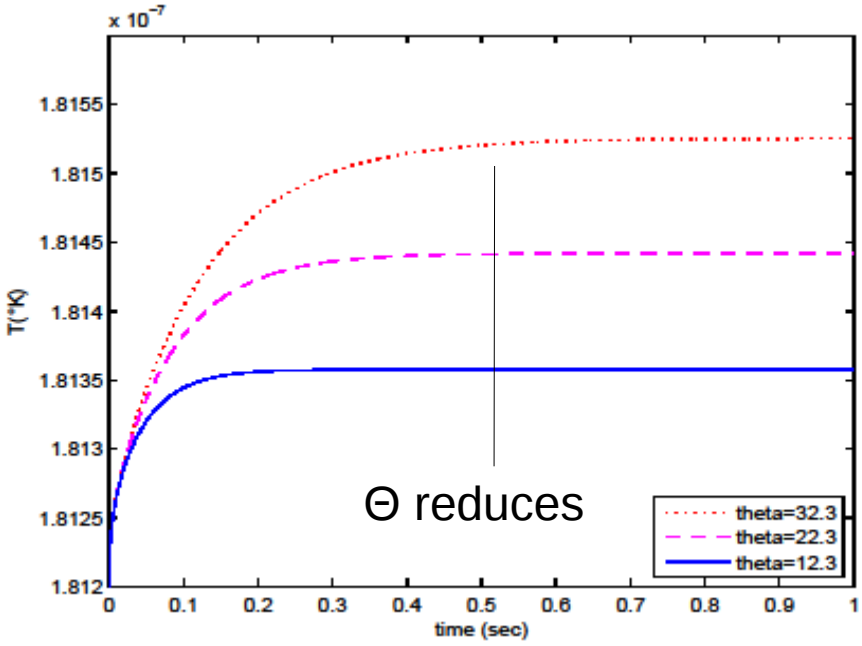


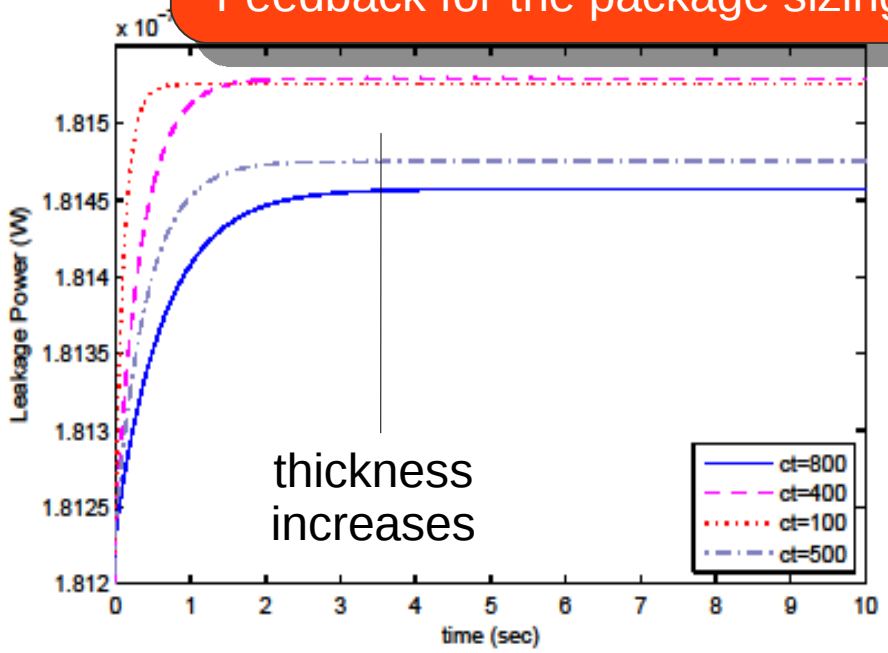
- Temperature-aware power characterization are used in the PCBs

Exploiting the Thermal Feedback

- Electro-thermal coupling effect for different heat spreading technologies
  - [Θ] = K/W → temperature difference between the environment and the heat spreader to dissipate 1W (thermal resistance)
  - [ct] = um → thickness of the spreader

Simulation over time
Maximum temperature analysis
Feedback for the package sizing





Component Interaction Analysis

- Analyze the impact of a component on the others in order to evaluate system level power/thermal management policies

3 power domains: Cores1/2, Configurable Logic, SMI

1	C1/C2	CL	SMI
ON	X	X	X
CG			
PG			

2	C1/C2	CL	SMI
ON			
CG			X
PG	X	X	

3	C1/C2	CL	SMI
ON	X	X	
CG			
PG			X

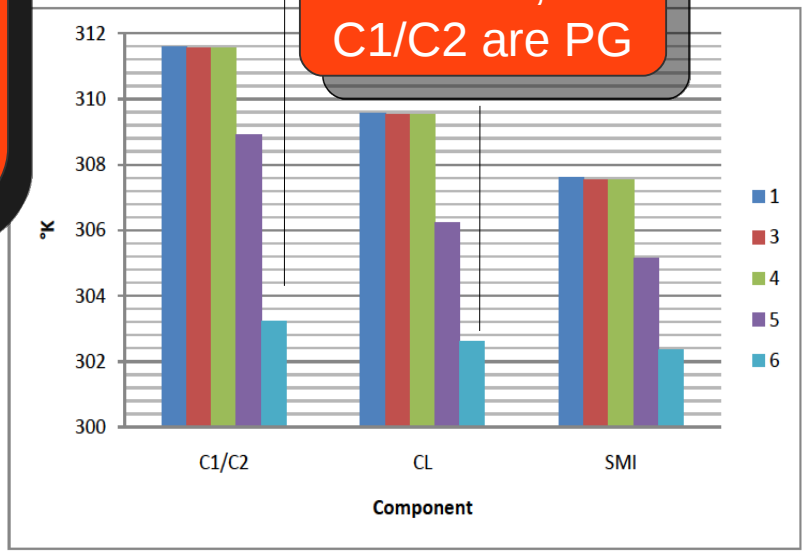
4	C1/C2	CL	SMI
ON	X	X	
CG			X
PG			

5	C1/C2	CL	SMI
ON	X		
CG			X
PG		X	

6	C1/C2	CL	SMI
ON		X	
CG			X
PG	X		

effect of PG

CL is ON, but C1/C2 are PG



SMI Leakage increase due to other components in some configuration

Configuration	***4***	***5***	***6***
Leakage increase	36%	23%	12%

Conclusions

- Temperature matters... several figures of merit are affected (Performance, Power, Reliability)
- Thermal aware design has become a must
- Estimating temperature in the earlier design stages is of paramount importance
- Integrated power/thermal estimators are now required
  - Heterogeneous power information (from system to physical level)
  - Link power and physical information to tech dependent thermal libraries
  - Thermal feedback to drive thermal-aware design strategies