

GLSVLSI 2010 Program

Sunday, May 16th, 2010

Special Session: Design Issues and Applications in VLSI: 3:00pm – 6:15pm

Session Chair: Fabrizio Lombardi (*Northeastern University*)

NoC-based Reconfigurable Embedded System Design

Donatella Sciuto (*Politecnico di Milano, Italy*)

Microelectronic Neurosensor Arrays: Towards Implantable Brain Communication Interfaces

Arto Nurmikko (*Brown University*)

Microprocessor Power Impacts

Mondira (Mandy) Pant (*Intel*)

Reception: 6:15pm – 8:00pm

Monday, May 17th, 2010

Opening: 8:00am – 8:30am

Session 1.1: CAD I: 8:30am – 10:30am

Session Chair: Mondira Pant (*Intel Corporation*)

A New Physical Routing Approach for Robust Bundled Signaling on NoC Links

Mohammad Reza Kakoei (*University of Bologna*)

Igor Loi (*University of Bologna*)

Luca Benini (*University of Bologna*)

Bus Via Reduction Based on Floorplan Revising

Ou He (*Tsinghua University*)

Sheqin Dong (*Tsinghua University*)

Jinian Bian (*Tsinghua University*)

Sotoshi Goto (*Waseda University*)

Chung-Kuan Cheng (*University of California, San Diego*)

Timing-Driven Variation-Aware Nonuniform Clock Mesh Synthesis

Ameer Abdelhadi (*Technion - Israel Institute of Technology*)

Ran Ginosar (*Technion - Israel Institute of Technology*)

Avinoam Kolodny (*Technion - Israel Institute of Technology*)

Eby G. Friedman (*Technion - Israel Institute of Technology*)

Scaling Power/Ground Solvers on Multi-Core with Memory Bandwidth Awareness

Jin Shi (*Tsinghua University*)

Yici Cai (*Tsinghua University*)

Bus-Pin-Aware Bus-Driven Floorplanning

Bo-Shiun Wu (*National Cheng Kung University*)

Tsung-Yi Ho (*National Cheng Kung University*)

Session 1.2: VLSI Circuits I: 8:30am – 10:30am

Session Chair: Emre Salman (*University of Rochester*)

8Gb/s Capacitive Low Power and High Speed 4-PWAM Transceiver Design

Young Bok Kim (*Northeastern University*)

Yong-Bin Kim (*Northeastern University*)

Fabrizio Lombardi (*Northeastern University*)

A Low Power, Variable Resolution Two-Step Flash ADC

Mahesh Kumar Adimulam (*Birla Institute of Technology and Science*)

Krishna Kumar Movva (*Birla Institute of Technology and Science*)

Sreehari Veeramachaneni (*Birla Institute of Technology and Science*)

N. Moorthy Muthukrishnan (*Birla Institute of Technology and Science*)

M. B. Srinivas (*Birla Institute of Technology and Science*)

A Low-offset High-speed Double-tail Dual-rail Dynamic Latched Comparator

HeungJun Jeon (*Northeastern University*)

Yong-Bin Kim (*Northeastern University*)

Via Configurable Three-Input Lookup-Tables for Structured ASICs

Yu-Chen Chen (*Yuan Ze University*)

Hou-Yu Pang (*Yuan Ze University*)

Kuen-Wen Lin (*Yuan Ze University*)

Rung-Bin Lin (*Yuan Ze University*)

Hui-Hsiang Tung (*Yuan Ze University*)

Shih-Chieh Su (*Ming Chuan University*)

Variation Tolerant 9T SRAM Cell Design

Sreeharsha Tavva (*Rochester Institute of Technology*)

Dhiresesha Kudithipudi (*Rochester Institute of Technology*)

Session 1.3: Testing I: 8:30am – 10:30am

Session Chair: Rui Tang (*Sun Microsystems - Oracle*)

Stochastic Computational Models for Accurate Reliability Evaluation of Logic Circuits

Hao Chen (*University of Alberta*)

Jie Han (*University of Alberta*)

A Multi-Level Approach to Reduce the Impact of NBTI on Processor Functional Units

Taniya Siddiqua (*University of Virginia*)

Sudhanva Gurumurthi (*University of Virginia*)

Graph Theoretic Approach for Scan Cell Reordering to Minimize Peak Shift Power

Jaynarayan T. Tudu (*Indian Institute of Science*)

Erik Larsson (*Linkoping University*)

Virendra Singh (*Indian Institute of Science*)

Hideo Fujiwara (*Nara Institute of Science and Technology*)

Gating Internal Nodes to Reduce Power During Scan Shift

Dheepakumaran Jayaraman (*Southern Illinois University, Carbondale*)

Rajamani Sethuram (*Qualcomm Inc.*)

Spyros Tragoudas (*Southern Illinois University, Carbondale*)

Software Adaptation in Quality Sensitive Applications to Deal with Hardware Variability

Aashish Pant (*University of California, Los Angeles*)

Puneet Gupta (*University of California, Los Angeles*)

Mihaela van der Schaar (*University of California, Los Angeles*)

Break: 10:30am – 11:00am

Poster Session I: 11:00am – 12:30pm

Session Chairs: Enrico Macii (*Politecnico di Torino*)

David Atienza (*EPFL*)

Write Activity Reduction on Flash Main Memory Via Smart Victim Cache

Liang Shi (*University of Science and Technology of China, City University of Hong Kong*)

Chun Jason Xue (*City University of Hong Kong*)

Jingtong Hu (*University of Texas at Dallas*)

Wei-Che Tseng (*University of Texas at Dallas*)

Xuehai Zhou (*University of Science and Technology of China*)

Edwin H.-M. Sha (*University of Texas at Dallas*)

Aging Effects of Leakage Optimizations for Caches

Andrea Calimera (*Politecnico di Torino*)

Mirko Loghi (*Università di Udine*)

Enrico Macii (*Politecnico di Torino*)

Massimo Poncino (*Politecnico di Torino*)

Thermal-Aware Floorplanning Exploration for 3D Multi-Core Architectures

David Cuesta (*Complutense University*)

Jose Ayala (*Complutense University*)

Jose Hidalgo (*Complutense University*)

Massimo Poncino (*Politecnico di Torino*)

Andrea Acquaviva (*Politecnico di Torino*)

Enrico Macii (*Politecnico di Torino*)

A Mask Double Patterning Technique Using Litho Simulation By Wavelet Transform

Rance Rodrigues (*University of Massachusetts at Amherst*)

Sandip Kundu (*University of Massachusetts at Amherst*)

An Effective Approach for Large Scale Floorplanning

Ameya R. Agnihotri (*SUNY Binghamton*)

Satoshi Ono (*SUNY Binghamton*)

Patrick H. Madden (*SUNY Binghamton*)

A Novel Resource Sharing Model and High-Level Synthesis for Delay Variability-Tolerant Datapaths

Keisuke Inoue (*Japan Advanced Institute of Science and Technology*)

Mineo Kaneko (*Japan Advanced Institute of Science and Technology*)

A Revisit to Voltage Partitioning Problem

Tao Lin (*Tsinghua University*)

Sheqin Dong (*Tsinghua University*)

Bei Yu (*Tsinghua University*)

Song Chen (*Waseda University*)

Satoshi Goto (*Waseda University*)

Resource-Constrained Timing-Driven Link Insertion for Critical Delay Reduction

Jin-Tai Yan (*Chung-Hua University*)

Zhi-Wei Chen (*Chung-Hua University*)

Boolean Satisfiability on a Graphics Processor

Kanupriya Gulati (*Texas A&M University*)

Sunil P. Khatri (*Texas A&M University*)

Pattern Grading for Testing Critical Paths Considering Power Supply Noise and Crosstalk Using a Layout-Aware Quality Metric

Junxia Ma (*University of Connecticut*)

Jeremy Lee (*University of Connecticut*)

Mohammad Tehranipoor (*University of Connecticut*)

Nisar Ahmed (*Texas Instruments, Inc.*)
Patrick Girard (*LIRMM, Université de Montpellier II / CNRS*)

Improving the Testability and Reliability of Sequential Circuits with Invariant Logic

Nuno Alves (*Brown University*)
Kundan Nepal (*Bucknell University*)
Jennifer Dworak (*Brown University*)
R. Iris Bahar (*Brown University*)

Deterministic Broadside Test Generation for Transition Path Delay Faults

Bo Yao (*Purdue University*)
Irith Pomeranz (*Purdue University*)
Sudhakar M. Reddy (*University of Iowa*)

A Delay Measurement Method Using a Shrinking Clock Signal

Jae Wook Lee (*The University of Texas at Austin*)
Ji Hwan Chun (*The University of Texas at Austin*)
Jacob A. Abraham (*The University of Texas at Austin*)

Energy-Efficient Redundant Execution for Chip Multiprocessors

Pramod Subramanyan (*Indian Institute of Science*)
Virendra Singh (*Indian Institute of Science*)
Kewal K. Saluja (*University of Wisconsin-Madison*)
Erik Larsson (*Linköping University*)

On-Die Sensors for Measuring Process and Environmental Variations in Integrated Circuits

Kanak Agarwal (*IBM Corporation*)

Cost Aware Fault Tolerant Logic Synthesis in Presence of Soft Errors

Xin He (*University of California, Riverside*)
Afshin Abdollahi (*University of California, Riverside*)

Design of Embedded MRAM Macros for Memory-in-Logic Applications

Sumanta Chaudhuri (*CNRS/University Paris Sud 11*)
Weisheng Zhao (*CNRS/University Paris Sud 11*)
Jacques-Olivier Klein (*University Paris Sud 11/CNRS*)
Claude Chappert (*CNRS/University Paris Sud 11*)
Pascale Mazoyer (*STMicroelectronics*)

Topology Impact on the Room Temperature Performance of THz-Range Ballistic Deflection Transistors

Vikas K. Kaushal (*University of Massachusetts, Lowell*)
Ignacio Iñiguez-de-la-Torre (*University of Massachusetts, Lowell*)
Martin Margala (*University of Massachusetts, Lowell*)

Performance Assessment of Analog Circuits with Carbon Nanotube FET (CNFET)

Janardhanan S. Ajit (*Northeastern University*)
Yong-Bin Kim (*Northeastern University*)
Minsu Choi (*Missouri University of Science & Technology*)

Read-Out Schemes for a CNTFET-Based Crossbar Memory

Sheng Lin (*Northeastern University*)
Yong Bin Kim (*Northeastern University*)
Fabrizio Lombardi (*Northeastern University*)

Lunch: 12:30pm – 2:00pm

Invited Speaker 2: 2:00pm – 3:00pm

Session Chair: Iris Bahar (*Brown University*)

Synthetic Biology: From Modules to Systems

Ron Weiss (*Massachusetts Institute of Technology*)

Break: 3:00pm – 3:30pm

Session 2.1: CAD II: 3:30pm – 5:30pm

Session Chair: Sandip Kundu (*University of Massachusetts*)

Dominant Critical Gate Identification for Power and Yield Optimization in Logic Circuits

Mihir Choudhury (*Rice University*)

Masoud Rostami (*Rice University*)

Kartik Mohanram (*Rice University*)

Logic Synthesis for Low Power Using Clock Gating and Rewiring

Tak-Kei Lam (*The Chinese University of Hong Kong*)

Steve Yang (*ICScape, Inc.*)

Wai-Chung Tang (*The Chinese University of Hong Kong*)

Yu-Liang Wu (*The Chinese University of Hong Kong*)

Dynamically Resizable Binary Decision Diagrams (Page 185)

Stergios Stergiou (*Fujitsu Laboratories of America*)

Jawahar Jain (*Fujitsu Laboratories of America*)

Fast Instruction Cache Modeling for Approximate Timed HW/SW Co-Simulation

Juan Castillo (*University of Cantabria*)

Hector Posadas (*University of Cantabria*)

Eugenio Villar (*University of Cantabria*)

Marcos Martínez (*Design of Systems on Silicon S.A.*)

Clock Skew Reduction by Self-Compensating Manufacturing Variability with On-Chip Sensors

Shinya Abe (*Osaka University & JST, CREST*)

Ken-ichi Shinkai (*Osaka University*)

Masanori Hashimoto (*Osaka University & JST, CREST*)

Takao Onoye (*Osaka University & JST, CREST*)

Session 2.2: Low Power I: 3:30pm – 5:30pm

Session Chair: Ayse K. Coskun (*Boston University*)

Online Convex Optimization-Based Algorithm for Thermal Management of MPSoCs

Francesco Zanini (*Ecole Polytechnique Fédérale de Lausanne*)

David Atienza (*Ecole Polytechnique Fédérale de Lausanne*)

Giovanni De Micheli (*Ecole Polytechnique Fédérale de Lausanne*)

Stephen P. Boyd (*Stanford University*)

Overscaling-friendly Timing Speculation Architectures

John Sartori (*University of Illinois*)

Rakesh Kumar (*University of Illinois*)

A Model to Exploit Power-Performance Efficiency in Superscalar Processors Via Structure Resizing

Omer Khan (*University of Massachusetts, Amherst*)

Sandip Kundu (*University of Massachusetts, Amherst*)

Thermal-Aware Compilation for System-on-Chip Processing Architectures

Mohamed M. Sabry (*Ecole Polytechnique Fédérale de Lausanne*)

José L. Ayala (*Complutense University of Madrid*)

David Atienza (*Ecole Polytechnique Fédérale de Lausanne*)

A Linear Statistical Analysis for Full-Chip Leakage Power with Spatial Correlation

Ruijing Shen (*University of California, Riverside*)

Sheldon X.-D. Tan (*University of California, Riverside*)

Jinjun Xiong (*IBM Thomas J. Watson Research Center*)

Session 2.3: VLSI Design and Post-CMOS Technology: 3:30pm – 5:30pm

Session Chair: Smita Krishnaswamy (*IBM T.J. Watson Research Center*)

Semi-Analytical Model for Schottky-Barrier Carbon Nanotube and Graphene Nanoribbon Transistors

Xuebei Yang (*Rice University*)

Gianluca Fiori (*University of Pisa*)

Giuseppe Iannaccone (*University of Pisa*)

Kartik Mohanram (*Rice University*)

Lightweight Runtime Control Flow Analysis for Adaptive Loop Caching

Marisha Rawlins (*University of Florida*)

Ann Gordon-Ross (*University of Florida*)

Low Power Nanoscale Buffer Management for Network on Chip Routers

Suman K. Mandal (*Texas A&M University*)

Ron Denton (*Texas A&M University*)

Saraju P. Mohanty (*University of North Texas*)

Rabi N. Mahapatra (*Texas A&M University*)

TURBONFS: Turbo Nand Flash Search

Shruti Vyas (*University of Massachusetts*)

Aswin Sreedhar (*University of Massachusetts*)

Sandip Kundu (*University of Massachusetts*)

Write Buffer-Oriented Energy Reduction in the L1 Data Cache of Two-Level Caches for the Embedded System

Soontae Kim (*Korea Advanced Institute of Science and Technology*)

Jongmin Lee (*Korea Advanced Institute of Science and Technology*)

Banquet Dinner: 6:30pm – 8:30pm

Tuesday, May 18th, 2010

Session 3.1: Emerging Technology: 8:30am – 10:30am

Session Chair: Baris Taskin (*Drexel University*)

Graphene Tunneling FET and Its Applications in Low-Power Circuit Design

Xuebei Yang (*Rice University*)

Jyotsna Chauhan (*University of Florida*)

Jing Guo (*University of Florida*)

Kartik Mohanram (*Rice University*)

Scalable Identification of Threshold Logic Functions

Ashok kumar Palaniswamy (*Southern Illinois University*)

Manoj kumar Goparaju (*Southern Illinois University*)

Spyros Tragoudas (*Southern Illinois University*)

Manufacturing Yield of QCA Circuits by Synthesized DNA Self-Assembled Templates

Xiaojun Ma (*Northeastern University*)

Masoud Hashempour (*Northeastern University*)

Lei Wang (*University of Connecticut*)

Fabrizio Lombardi (*Northeastern University*)

Numerical Queue Solution of Thermal Noise-Induced Soft Errors in Subthreshold CMOS Devices

Pooya Jannaty (*Brown University*)

Florian C. Sabou (*Brown University*)

R. Iris Bahar (*Brown University*)

Joseph Mundy (*Brown University*)

William R. Patterson (*Brown University*)

Alexander Zaslavsky (*Brown University*)

Design Considerations for Variation Tolerant Multilevel CMOS/Nano Memristor Memory

Harika Manem (*New York University*)

Garrett S. Rose (*New York University*)

Xiaoli He (*University at Albany*)

Wei Wang (*University at Albany*)

Session 3.2: Special Session I: System-Level SoC Design: 8:30am – 10:30am

Session Chair: Yong-Bin Kim (*Northeastern University*)

An Integrated Thermal Estimation Framework for Industrial Embedded Platforms

Andrea Acquaviva (*Politecnico di Torino*)

Andrea Calimera (*Politecnico di Torino*)

Alberto Macii (*Politecnico di Torino*)

Massimo Poncino (*Politecnico di Torino*)

Enrico Macii (*Politecnico di Torino*)

Matteo Giaconia (*STMicroelectronics*)

Claudio Parrella (*STMicroelectronics*)

Power-Efficient, Reliable Microprocessor Architectures: Modeling and Design Methods

Pradip Bose (*IBM T.J. Watson Research Center*)

Alper Buyuktosunoglu (*IBM T.J. Watson Research Center*)

Chen-Yong Cher (*IBM T.J. Watson Research Center*)

John A. Darringer (*IBM T.J. Watson Research Center*)

Meeta S. Gupta (*IBM T.J. Watson Research Center*)

Hendrik Hamann (*IBM T.J. Watson Research Center*)

Hans Jacobson (*IBM T.J. Watson Research Center*)

Prabhakar N. Kudva (*IBM T.J. Watson Research Center*)

Eren Kursun (*IBM T.J. Watson Research Center*)

Niti Madan (*IBM T.J. Watson Research Center*)

Indira Nair (*IBM T.J. Watson Research Center*)

Jude A. Rivers (*IBM T.J. Watson Research Center*)

Jeonghee Shin (*IBM T.J. Watson Research Center*)

Alan J. Weger (*IBM T.J. Watson Research Center*)

Victor Zyuban (*IBM T.J. Watson Research Center*)

Performance and Energy Trade-offs Analysis of L2 On-Chip Cache Architectures for Embedded MPSoCs

Mohamed M. Sabry (*Ecole Polytechnique Fédérale de Lausanne*)

Martino Ruggiero (*Ecole Polytechnique Fédérale de Lausanne & University of Bologna*)

Pablo G. Del Valle (*Ecole Polytechnique Fédérale de Lausanne & DACYA, UCM*)

A Virtual Platform Environment for Exploring Power, Thermal and Reliability Management Control Strategies in High-Performance Multicores

Andrea Bartolini (*University of Bologna*)

Matteo Cacciari (*University of Bologna*)

Andrea Tilli (*University of Bologna*)

Luca Benini (*University of Bologna*)

Matthias Gries (*Intel Laboratories*)

Challenges and Methodologies for Efficient Power Budgeting Across the Die

Pinkesh J. Shah (*Intel Corporation*)

Yoni Aizik (*Intel Corporation, Israel*)

Muhammad Mhameed (*Intel Corporation, Israel*)

Gila Kamhi (*Intel Corporation, Israel*)

Session 3.3: VLSI Design: 8:30am – 10:30am

Session Chair: Jose L. Ayala (*Complutense University*)

A DOE-ILP Assisted Conjugate-Gradient Based Power and Stability Optimization in High-K Nano-CMOS SRAM

Garima Thakral (*University of North Texas*)

Saraju P. Mohanty (*University of North Texas*)

Dhruva Ghai (*University of North Texas*)

Dhiraj K. Pradhan (*University of Bristol*)

Line Width Optimization for Interdigitated Power/Ground Networks

Renatas Jakushokas (*University of Rochester*)

Eby G. Friedman (*University of Rochester*)

Thermal-Aware Voltage Droop Compensation for Multi-core Architectures

Jia Zhao (*University of Massachusetts*)

Basab Datta (*University of Massachusetts*)

Wayne Burleson (*University of Massachusetts*)

Russell Tessier (*University of Massachusetts*)

Analysis and Mitigation of NBTI-Impact on PVT Variability in Repeated Global Interconnect Performance

Basab Datta (*University of Massachusetts-Amherst*)

Wayne Burleson (*University of Massachusetts-Amherst*)

Collaborative Voltage Scaling with Online STA and Variable-Latency Datapath

Tay-Jyi Lin (*Industrial Technology Research Institute & National Chiao Tung University*)

Pi-Cheng Hsiao (*Industrial Technology Research Institute*)

Chi-Hung Lin (*Industrial Technology Research Institute*)

Shu-Chang Kuo (*Industrial Technology Research Institute*)

Chou-Kun Lin (*Industrial Technology Research Institute*)

Yu-Ting Kuo (*National Chiao Tung University*)

Chih-Wei Liu (*National Chiao Tung University*)

Yuan-Hua Chu (*Industrial Technology Research Institute*)

Break: 10:30am – 11:00am

Poster Session II: 11:00am – 12:30pm

Session Chair: Saraju P. Mohanty (*University of North Texas*)

AOP-Based High-Level Power Estimation in SystemC

Feng Liu (*National Lab of Parallel Distributed Processing, Hunan, China*)

Qingping Tan (*National Lab of Parallel Distributed Processing, Hunan, China*)

Xiaoyu Song (*Portland State University*)

Naeem Abbasi (*Concordia University*)

A Novel Crosstalk Quantitative Approach for Simultaneously Reducing Power, Noise, and Delay Based on Bus-invert Encoding Schemes

Shanq-Jang Ruan (*National Taiwan University of Science and Technology*)

Tsang-Chi Kan (*National Taiwan University of Science and Technology*)

Jih-Chieh Hsu (*National Taiwan University of Science and Technology*)

The Challenges of Implementing Fine-Grained Power Gating

Anja Niedermeier (*Norwegian University of Science and Technology*)

Kjetil Svarstad (*Norwegian University of Science and Technology*)

Frank Bouwens (*Holst Centre / Stichting IMEC-NL*)

Jos Hulzink (*Holst Centre / Stichting IMEC-NL*)

Jos Huiskens (*Holst Centre / Stichting IMEC-NL*)

Performance and Energy Efficient Cache Migration Approach for Thermal Management in Embedded Systems

Raid Ayoub (*University of California, San Diego*)

Alex Orailoglu (*University of California, San Diego*)

Performance Enhancement of Subthreshold Circuits Using Substrate Biasing and Charge-Boosting Buffers

Sumanth Amarchinta (*Rochester Institute of Technology*)

Dhiresha Kudithipudi (*Rochester Institute of Technology*)

Reliability Analysis of Power Gated SRAM Under Combined Effects of NBTI and PBTlin Nano-Scale CMOS

Anuj Pushkarna (*San Francisco State University*)

Hamid Mahmoodi (*San Francisco State University*)

On-Chip Point-of-Load Voltage Regulator for Distributed Power Supplies

Selçuk Köse (*University of Rochester*)

Eby G. Friedman (*University of Rochester*)

VLSI Implementation of a Non-Linear Feedback Shift Register for High-Speed Cryptography Applications

Pey-Chang Kent Lin (*Texas A&M University*)

Sunil P. Khatri (*Texas A&M University*)

Out-of-Order Issue Logic Using Sorting Networks

Siddhesh S. Mhambrey (*Arizona State University*)

Lawrence T. Clark (*Arizona State University*)

Satendra Kumar Maurya (*Arizona State University*)

Krzysztof S. Berezowski (*Grenoble-INP*)

On-Chip Power Supply Noise and Its Implications on Timing

Lars J. Svensson (*Chalmers University of Technology*)

Johnny Pihl (*Atmel Norway AS*)

Daniel A. Andersson (*Atmel Norway AS*)

Per Larsson-Edefors (*Chalmers University of Technology*)

Characteristics of MS-CMOS Logic in Sub-32nm Technologies

Kagan Irez (*Columbia University*)

Jiaping Hu (*Columbia University*)

Charles A. Zukowski (*Columbia University*)

A Self-Adaptive Scheduler for Asymmetric Multi-Cores

Omer Khan (*University of Massachusetts, Amherst*)

Sandip Kundu (*University of Massachusetts, Amherst*)

Context-Aware TLB Preloading for Interference Reduction in Embedded Multi-Tasked Systems

Ilya Chukhman (*University of Maryland*)

Peter Petrov (*University of Maryland*)

Design of Self Correcting Radiation Hardened Digital Circuits Using Decoupled Ground Bus

Sohan Purohit (*University of Massachusetts, Lowell*)

Sai Rahul Chalamalasetti (*University of Massachusetts, Lowell*)

Martin Margala (*University of Massachusetts, Lowell*)

A Novel Multi-Objective Instruction Synthesis Flow for Application-Specific Instruction Set Processors

Hai Lin (*University of Connecticut*)

Yunsi Fei (*University of Connecticut*)

Electromagnetic Interaction of On-Chip Antennas and CMOS Metal Layers for Wireless IC Interconnects

Ankit More (*Drexel University*)

Baris Taskin (*Drexel University*)

Lunch: 12:30pm – 2:00pm

Session 4.1: CAD III: 2:00pm – 4:00pm

Session Chair: Kundan Nepal (*Bucknell University*)

Ordered Escape Routing Via Routability-Driven Pin Assignment

Jin-Tai Yan (*Chung-Hua University*)

Chung-Wei Ke (*Chung-Hua University*)

Zhi-Wei Chen (*Chung-Hua University*)

Temperature-Constrained Fixed-Outline Floorplanning for Die-Stacking System-in-Package Design

De-Yu Liu (*National Tsing Hua University*)

Wai-Kei Mak (*National Tsing Hua University*)

Ting-Chi Wang (*National Tsing Hua University*)

Performance-Constrained Template-Driven Retargeting for Analog and RF Layouts

Zheng Liu (*Memorial University of Newfoundland*)

Lihong Zhang (*Memorial University of Newfoundland*)

Wirelength-Driven Force-Directed 3D FPGA Placement

Wentao Sui (*Tsinghua University*)

Sheqin Dong (*Tsinghua University*)

Jinian Bian (*Tsinghua University*)

A Novel Droplet Routing Algorithm for Digital Microfluidic Biochips

Pranab Roy (*Bengal Engineering and Science University*)

Hafizur Rahaman (*Bengal Engineering and Science University*)

Parthasarathi Dasgupta (*Indian Institute of Management, Calcutta*)

Session 4.2: VLSI Circuits II: 2:00pm – 4:00pm

Session Chair: Erik Brunvand (*University of Utah*)

Methodology to Achieve Higher Tolerance to Delay Variations in Synchronous Circuits

Emre Salman (*University of Rochester*)

Eby G. Friedman (*University of Rochester*)

Circuit-Level NBTI Macro-Models for Collaborative Reliability Monitoring

Basab Datta (*University of Massachusetts, Amherst*)

Wayne Burleson (*University of Massachusetts, Amherst*)

Low-Power Side-Channel Attack-Resistant Asynchronous S-Box Design for AES Cryptosystems

Jun Wu (*Missouri University of Science & Technology*)

Yong-Bin Kim (*Northeastern University*)

Minsu Choi (*Missouri University of Science & Technology*)

Enhancing Debugging of Multiple Missing Control Errors in Reversible Logic

Jean Christoph Jung (*Institute for Computer Science, Germany*)

Stefan Frehse (*Institute for Computer Science, Germany*)

Robert Wille (*Institute for Computer Science, Germany*)

Rolf Drechsler (*Institute for Computer Science, Germany*)

Algorithm and Hardware Complexity Reduction Techniques for K-best Sphere Decoders

Nariman Moezzi-Madani (*North Carolina State University*)

Thorlindur Thorolfsson (*North Carolina State University*)

William Rhett Davis (*North Carolina State University*)

Closing Remarks: 4:00pm – 4:30pm