GLSVLSI 08 Advance Program

Sunday May 4th, 2008

1.00 pm-5.00 pm: Tutorials
"Technology, CAD Tools, and Designs for Emerging 3D Integration Technology"
Presenters:
Syed M. Alam, Freescale Semiconductor
Mike Ignatowski, IBM TJ Watson Research Center
Yuan Xie, Pennsylvania State University

Monday May 5th, 2008

8.00 am-8.15 am: Opening Session

8.15 am-9.15 am: Plenary Talk
"Directions for Silicon Technology as We Approach the End of CMOS Scaling"
Speaker: Tak H Ning, IBM TJ Watson Research Center

9.30 am-10.50 am Session 1A: Modeling and Design under Variations
Session Chair: D. Atienza, LSI/Ecole Polytechnique Federale de Lausanne (EPFL)

Temperature-Insensitive Synthesis Using Multi-Vt Libraries (L)
Andrea Calimera, Iris Bahar, Enrico Macii and Massimo Poncino

A Formula of STI CMP Design Rule (L)
Min-Chun Tsai.

Considering Possible Opens in Non-tree Topology Wire Delay Calculation (L)
Philipp Panitz, Markus Olbrich, Erich Barke, Markus Buehler and Juergen Koehl

Variational Capacitance Modeling Using Orthogonal Polynomial Method (L)
Jian Cui, Sheldon Tan, Ruijing Shen and Wenjian Yu

9.30 am-10.50 am Session 1B: Addressing Emerging Technology Issues in VLSI Circuits
Session Chair: S. Alam, Freescale Semiconductor

NBTI-Aware Flip-Flop Characterization and Design (L)
Hamed Abrishami, Safar Hatami and Massoud Pedram

On-Die CMOS Voltage Droop Detection and Dynamic Compensation (L)
Matthew Holtz, Seetharam Narasimhan and Swarup Bhunia

Collaborative Sensing of On-Chip Wire Temperatures using Interconnect based Ring Oscillators (L)
Basab Datta and Wayne Burleson

A Process and Supply Variation Tolerant Nano-CMOS Low Voltage, High Speed, A/D Converter for System-on-Chip (L)
Dhruva Ghai, Saraju Mohanty and Elias Kougianos

Coffee Break-10.50 am-11.00 am.

11:00 am-12:20 pm Session 2A: Cryptography and Architecture
Session Chair: M. Bayoumi, University of Louisiana at Lafayette

A GF(p) Elliptic Curve Group Operator Resistant against Side Channel Attacks (L)
Santosh Ghosh

Reconfigurable Solutions for Very-Long Arithmetic with Applications in Cryptography (L)
Ambrose Chu, Scott Miller and Mihai Sima

Fast Composite Field S-Box Architectures for Advanced Encryption Standard (L)
Renfei Liu and Keshab Parhi

A Table-based Method for Single-Pass Cache Optimization (L)
Pablo Viana, Ann Gordon-Ross, Edna Barros and Frank Vahid

11:00 am-12:20 pm Session 2B: System-Level Testing, Verification and Design
Session Chair: S. Mohanty, University of North Texas

Using Unsatisfiable Cores to Debug Multiple Design Errors (L)
Andre Suelflow, Goerschwin Fey, Roderick Bloem and Rolf Drechsler

A Novel Test-Data Compression Technique using Application-Aware Bitmask and Dictionary Selection Methods (L)
Kanad Basu and Prabhat Mishra

HyMacs: Hybrid Memory Access Optimization based on Custom-instruction Scheduling (L)
Kang Zhao, Jinian Bian, Sheqin Dong, Yang Song and Satoshi Goto

Automated Formal Verification of Scheduling with SpeculativeCode Motions (S)
Youngsik Kim and Nazanin Mansouri

Statistical Timing Analysis of flip-flops Considering Codependent Setup and Hold Times (S)
Safar Hatami, Hamed Abrishami and Massoud Pedram

Lunch 12:30 pm- 2.00 pm

2:00 pm-3:30 pm Poster Session 1
Session Chair: T. Theocharides, University of Cyprus

Compressor Trees for Decimal Partial Product Reduction
Ivan Castellanos and James Stine

Generic Sub-Space Algorithm for Generating Reduced Order Models of Linear Time Varying VLSI Circuits
Ravindra Jayanthi and Srinivas Mandalika

A High-Speed Radix-4 Multiplexer-Based Array Multiplier
Dimitris Bekiaris, Kiamal Pekmestzi and Chris Papachristou

A Robust, Fast Pulsed Flip-Flop Design
Arunprasad Venkatraman, Rajesh Garg and Sunil Khatri

Design of High efficiency DC-DC converter using Low power buffer and On-Chip Compensation
Daewoong Cho, Seungchan Park, Kyungoun Jang and Kwangsub Yoon

A New Technique in Design of Active RF CMOS Mixers for Low Flicker Noise and High Conversion Gain
Yarallah Koolivand, Morteza Alavi and Omid Shoaei

A Low Leakage 9T SRAM Cell for Ultra-Low Power Operation
Sheng Lim, Yong-Bin Kim and Fabrizio Lombardi

Recursion Flattening
Greg Stitt and Jason Villarreal

Quick Supply Current Waveform Estimation at Gate Level Using Existed Cell Library Information
Mu-Shun Lee, Chin-Hsun Lin, Chien-Nan Jimmy Liu and Shih-Che Lin

Coverage-driven Automatic Test Generation for UML Activity Diagrams
Mingsong Chen and Prabhat Mishra

Hardware/Software Partitioning with Multi-Version Implementation Exploration
Greg Stitt

Network Coding for Routability Improvement in FPGAs
Kanupriya Gulati and Sunil Khatri

Impact of Dummy Filling Techniques on Interconnect Capacitance and Planarization in Nano-Scale Process Technology
Arthur Nieuwoudt, Jamil Kawa and Yehia Massoud

Dynamic P/G Grid Topology Optimization Techniques for Low Power Design
Jin Shi, Yici Cai, Xianlong Hong and Sheldon X-D. Tan

Loop Scheduling and Assignment with Prefetching to Minimize Energy while Hiding Memory Latencies
Meikang Qiu

A Circuit Matrix Model Based Layout Aware Method for Module Selection and Synthesis of Analog Circuits
Almitra Pradhan and Ranga Vemuri

Delay Driven AIG Restructuring using Slack Budget Management
Andrew Ling, Jianwen Zhu and Stephen Brown

An analytical approach to placement legalization
Andrey Ayupov, Alexander Marchenko and Vladimir Tiourin

Coffee Break – 3.30 pm-3.40 pm.

3.40 pm-5.00 pm Session 3A: Low Power Circuits

Session Chair: M. Stan, University of Virginia

Simultaneous Optimization of Total Power, Crosstalk Noise, and Delay Under Uncertainty (L)
Nagarajan Ranganathan, Upavan Gupta and Venkatraman Mahalingam

Optimal Sleep Transistor Synthesis Under Timing and Area Constraints (L)
Ashoka Sathanur, Antonio Pullini, Luca Benini, Alberto Macii, Enrico Macii and Massimo Poncino

Energy Efficiency Bounds of Pulse-Encoded Buses (L)
Karthik Duraisami, Enrico Macii and Massimo Poncino

Implementation of Asynchronous Pipeline Circuits in Multi-Threshold CMOS Technologies (L)
Raghid Shreih and Maitham Shams

3:40 pm - 5:00 pm Session 3B: Modeling and Design of Advanced VLSI Circuits

Session Chair: A. Bhavnagarwala, IBM TJ Watson Research Center

Efficient Modeling and Design Methodology for Ultra-Low-Power Common-Gate RF Front-End (L)
Hamid Nejati, Tamer Ragheb and Yehia Massoud

Verifying Start-Up Conditions for a Ring Oscillator (L)
Mark Greenstreet and Suwen Yang

A Cost-Efficient Partially-Parallel Irregular LDPC Decoder Based on Sum-Delta Message Passing Algorithm (L)
Wen Ji, Yuta Abe, Takeshi Ikenaga and Satoshi Goto

Pipelined Network of PLA Based Circuit Design (S)
Suganth Paul, Rajesh Garg and Sunil Khatri

A Low-Power 12-Bit 80MHz CMOS DAC Using Pseudo-Segmentation (S)
Chanyang Joo, Soojae Kim and Kwangsub Yoon

6.30 pm-8.30 pm---Banquet

Tuesday 6th May, 2008

8.15 am-9.15 am: Plenary Talk

"Architectures for Distributed Smart Cameras**"**
Speaker: Wayne Wolf, Princeton University

9.30 am-10.50 am Session 4A: Emerging Technologies

Session Chair: F. Fummi, Universita` di Verona

SAT-based Equivalence Checking of Threshold Logic Designs for Nanotechnologies (L)
Yexin Zheng, Michael Hsiao and Chao Huang

Pair wise Decomposition of Toffoli Gates in a Quantum Circuit (L)
Nathan Scott and Gerhard W. Dueck

Design of Defect Tolerant Tile-based QCA Circuits (L)
Vamsi Vankamamidi and Fabrizio Lombardi

A Layout-aware Physical Design Method for Constructing Feasible QCA Circuits (S)
Mayur Bubna, Sudip Roy, Naresh Shenoy and Rajib Mall

A Hybrid CMOS/Nano FPGA Architecture built from Programmable Majority Logic Arrays (S)
Harika Manem, Peter Paliwoda and Garrett Rose

9.30 am-10.50 am Session 4B: Physical synthesis

Session Chair: S. Khatri, Texas A&M University

A Novel Performance Driven Power Gating Based on Distributed Sleep Transistor Network (L)
Liangpeng Guo, Yici Cai, Qiang Zhou, Le Kang and Xianlong Hong

A Practical Repeater Insertion Flow (L)
Nikolai Ryzhenko and Oleg Venger

Criticality History Guided FPGA Placement Algorithm for Timing Optimization (L)
Hao Li and Yue Zhuo

A Linear Programming Formulation for Security-Aware Gate Sizing (L)
Koustav Bhattacharya and Nagarajan Ranganathan

Coffee Break: 10.50 am-11.00 am

11:00 am -12:20 pm Session 5A: Testing and Resilient Circuits

Session Chair: F. Lombardi, Northeastern University

On efficient generation of instruction sequences to test for delay defects in a processor (L)
Sankar Gurumurthy, Ramtilak Vemu and Jacob Abraham

NBTI Resilient Circuits Using Adaptive Body Biasing (L)
Zhenyu(Jerry) Qi and Mircea Stan

A tool flow for predicting system level timing failures due to interconnect reliability degradation (L)
Jin Guo, Antonis Papanikolaou, Michele Stucchi, Kristof Croes, Zsolt Tokei and Francky Catthoor

Statistically Translating Low-Level Error Probabilities to Increase the Accuracy and Efficiency of Reliability Simulations in Hardware Description Languages (S)
Drew Ness and David Lilja

Improved Bit Error Rate Performance in Intra-Chip RF/Wireless Interconnect Systems (S)
Md. Sajjad Rahaman and Masud Chowdhury.

11:00 am -12:20 pm Session 5B: VLSI Design

Session Chair: N. Ranganathan, University of South Florida

Scalable and Fault-tolerant Network-on-Chip Design Using the Quartered Recursive Diagonal Torus Topology (L)
Xianfang Tan, Lei Zhang, Shankar Neelkrishnan, Mei Yang, Yingtao Jiang and Yulu Yang

A Lithography-friendly Structured ASIC Design Approach (L)
Salman Gopalani, Rajesh Garg, Sunil Khatri and Mosong Cheng

Efficient Tree topology for FPGA interconnect network (L)
Zied Marrakchi, Hayder Mrabet and Habib Mehrez

Assumers for High-Speed Single and Multi-Cycle On-chip Interconnect With Low Repeater Count (S)
Charbel Akl and Magdy Bayoumi

MLP Neural Network and On-line Backpropagation Learning Implementation in a Low-Cost FPGA (S)
Ernesto Ordonez-Cardenas and Rene de J Romero-Troncoso

Lunch 12.30 pm-2.00 p.m

2:00 pm-3:30 pm Poster Session 2
Session Chair: S. Mohanty, University of North Texas

Fast Bus Waveform Estimation at the Presence of Coupling Noise
Jingye Xu, Pervez Khaled and Masud Chowdhury

Mesh-of-Tree Deterministic Routing for Network-on-Chip Architecture
Santanu Kundu and Santanu Chattopadhyay

FPGA-Based Hardware/Software Co-design for Chirplet Signal Decomposition
Yufeng Lu, Erdal Oruklu and Jafar Saniie

Trends in Energy-efficiency and Robustness using Stochastic Sensor Network-on-a-Chip
Girish Varatkar, Sriram Narayanan, Naresh Shanbhag and Douglas Jones

Using Reiterative LFSR Based X-Masking to Increase Output Compression in Presence of Unknowns
Richard Putman

Efficient and Optimal Post-Layout Double-Cut Via Insertion by Network Relaxation and Min-Cost Maximum Flow
Lun-Chun Wei, Li-Da Huang, Hung-Ming Chen and Sarah Xu

Guided Test Generation for Isolation and Detection of Embedded Trojans in ICs
Mainak Banga, Maheshwar Chandrasekhar, Lei Fang and Michael S. Hsiao

Electrical Models for Vertical Carbon Nanotube Capacitors
Mark Budnik, Eric Johnson and Joshua Wood

In-Order Pulsed Charge Recycling in Off-Chip Data Buses
Kimish Patel, Wonbok Lee and Massoud Pedram

An Energy-Aware Co-Simulation Framework for the Design of Wireless Sensor Networks
Andrea Acquaviva, Franco Fummi, Giovanni Perbellini and Davide Quaglia

Phase-based Cache Reconfiguration for a Highly-Configurable Two-Level Cache Hierarchy
Ann Gordon-Ross, Jeremy Lau and Brad Calder

Instruction Cache Leakage Reduction by Changing Register Operands and Using Asymmetric SRAM Cells
Maziar Goudarzi and Tohru Ishihara

Experimental Study on Body-Biasing Layout Style -- Negligible Area Overhead Enables Sufficient Speed Controllability –
Koichi Hamamoto, Hiroshi Fuketa, Masanori Hashimoto, Yukio Mitsuyama and Takao Onoye

Full-Chip Leakage Current Estimation Based on Statistical Sampling Techniques
Shaobo Liu, Qinru Qiu and Qing Wu

A Low-Power Phase Change Memory Based Hybrid Cache Architecture
Prasanth Mangalagiri, Karthik Sarpatwari, Aditya Yanamandra, Vijaykrishnan Narayanan, Osama O Awadelkarim and Yuan Xie

Exploiting Frequent Opcode Locality for Power Efficient Instruction Cache
Yen-Jen Chang

Simultaneous Optimization of Memory Configuration and Code Allocation for Low Power Embedded Systems
Tadayuki Matsumura, Tohru Ishihara and Hiroto Yasuura

Simple and Accurate Method for Fast Static Current Estimation in CMOS Complex Gates with Interaction of Leakage Mechanisms
Paulo Butzen, Leomar Rosa Jr, Erasmo Chiappetta, Dionatan Moura, Andre Reis and Renato Ribas

Coffee Break – 3.30 pm-3.40 pm

3.40 pm-5.00 pm Session 6A: Low Power Architecture

Session Chair: Ann Gordon-Ross, University of Florida, Gainesville

Fast architecture-level thermal analysis for online thermal regulation (L)
Pu Liu, Wei Wu, Gengsheng Chen and Sheldon Tan

An analytical model for maximum on-chip temperature difference (L)
Shervin Sharifi and Tajana Simunic Rosing

Power Management of Variation Aware Chip Multiprocessors (S)
Abu Saad Papa and Madhu Mutyam

Low-Power Clock Distribution in a Multilayer Core 3D Microprocessor (S)
Venkatesh Arunachalam and Wayne Burleson

Energy Efficient Synchronization Techniques for Embedded Architectures (L)
Cesare Ferri, Amber Viescas, Tali Moreshet, R.Iris Bahar and Maurice Herlihy

3.40 pm-5.00 pm Session 6B: ADC and LDPC

Session Chair: S. Khatri, Texas A&M University

12bit 40MHz Pipelined ADC with Duty-Correction Circuit (L)
Jaeyong Lee, Sungil Jo and Kwangsub Yoon

Comparison of redundant architectures for two-step ADCs (L)
Gian Nicola Angotzi, Massimo Barbaro and Paul G.A, Jespers

Nonuniformly Quantized Min-Sum Decoder for Low-Density Parity-Check coder (L)
Daesun Oh and Keshab K. Parhi

Extended Layered Decoding of LDPC Codes (L)
Zhiqiang Cui and Zhongfeng Wang

5.00 pm -End Closing ceremony

Note: L- Long Paper; S- Short Paper