GLSVLSI 06 Advance Program

Sunday April 30, 2006

1:00-5:00 p.m. Tutorials

Monday May 1, 2006

8:00-8:15 a.m. Opening Session

8:15-10:15 a.m. Session 1: Emerging Technologies
Session Chair: Yuan Xie, Penn State

(**Best Student Paper**) Design Approaches for Hybrid CMOS/Molecular Memory based on Experimental Device Data
Garrett S. Rose, Adam C. Cabe, Nadine Gergel-Hackett, Nabanita Majumdar, Mircea R. Stan, John C. Bean, Lloyd R. Harriott, Yuxing Yao, and James M. Tour

Threshold/Majority Logic Synthesis and Concurrent Error Detection Targeting Nanoelectronic Implementations
Rui Zhang and Niraj K. Jha

Measurement and Characterization of Pattern Dependent Process Variations of Interconnect Resistance, Capacitance and Inductance in Nanometer Technologies
Xiaoning Qi, Alex Gyure, Yansheng Luo, Sam C. Lo, Mahmoud Shahram, and Kishore Singhal

Thermal Analysis of a 3D Die-Stacked High-Performance Microprocessor
Kiran Puttaswamy and Gabriel H. Loh

8:15-10:15a.m. Session 2: CAD for Embedded Systems
Session Chair: Dimitrios Velenis, IIT

HW/SW Partitioning Techniques for Multi-Mode Multi-Task Embedded Applications
Youngjun Kim and Taewhan Kim

ISS-Centric Modular HW/SW Co-Simulation
Mirko Loghi; Franco Fummi; Giovanni Perbellini; Massimo Poncino

An ILP Based Approach to Address Code Generation for Digital Signal Processors
Ozcan Ozturk, Mahmut Kandemir, and Suleyman Tosun

HW/SW Co-Verification of Embedded Systems using Bounded Model Checking
Daniel Grosse, Ulrich Kuehne, Rolf Drechsler

10:30a.m.-12:30p.m. Session 3: RF and Data Communication Circuits
Session Chair: Mona Hella, RPI

PWAM Signaling Scheme for High Speed Serial Link Tranceiver Design
Rui tang and Yong-Bin Kim

High Speed Differential Pulse-Width Control Loop Based on Frequency-to-Voltage Converters
Hung Tien Bui Yvon Savaria

Synthesis of Wideband Low Noise Amplifier
Abhishek Jajoo, Michael Sperling, Tamal Mukherjee

A 0.13um CMOS 10 Gb/s Current-Mode Class AB Serial Link Transmitter with Low Supply Voltage Sensitivity
M. Li and F. Yuan

10:30 a.m. -12:30 p.m. Session 4: Partitioning and Floorplanning
Session Chair: Mircea Stan, University of Virginia

Dominator-based Partitioning for Delay Optimization
David Baneres, Jordi Cortadella, Mike Kishinevsky

Does Partitioning Matter for 3D Floorplanning? - Empirical study on the importance of partitioning and impact of the number of vertical channels on the total wire length
Tan Yan, Qing Dong, Yasuhiro Takashima and Yoji Kajitani

Low-Power Clustering with Minimum Logic Replication for Coarse-grained, Antifuse based FPGAs
Chang Woo Kang and Massoud Pedram

Shuttle Mask Floorplanning with Modified Alpha-Restricted Grid
Royce L.S.Ching and Evangeline F.Y.Young

2:00 - 3:30 p.m. Poster Session 1
Session Chair: James Stine, Oklahoma State University

Delay and Power Estimation Models of Low-Swing Interconnects for Design Planning
Xiangyuan Liu and Shuming Chen

A Simulation Methodology for Reliability Analysis in Multi-Core SoCs
Ayse K. Coskun, Tajana Simunic-Rosing, Yusuf Leblebici, Giovanni De Micheli

Power Density Minimization for Highly-Associative Caches in Embedded Processors
Ja Chun Ku, Serkan Ozdemir, Gokhan Memik, Yehea Ismail

An Evaluation of the Impact of Gate Oxide Tunneling on Dual Vt Based Leakage Reduction Techniques
Lara D Oliver, Krishnendu Chakrabarty, and Hisham Z Massoud

Efficient Encoding for Address Buses with Temporal Redundancy for Simultaneous Area and Energy Reduction
Jiangjiang Liu, Krishnan Sundaresan, and Nihar R. Mahapatra

General TransistorLevel Methodology on VLSI LowPower Design
Zuying Luo

Delay and Peak Power Minimization for On-Chip Buses using Temporal Redundancy
K. Najeeb, Vishal Gupta, Madhu Mutyam and V. Kamakoti

Low-Noise High-Precision Operational Amplifier Using Vertical NPN Transistor in CMOS Technology
ZhiYuan Li, FengChang Lai, MingYan Yu

A New Power-Area Efficient 4-PAM Full-Clock CMOS Pre-Emphasis Transmitter for 10Gb/s Serial Links
F. Yuan

A Low–Power and High-Linear Double-Balanced Switch
Jun-Da Chen Zhi-Ming Lin

Nonlinearity Analysis in ISD CMOS LNA's Using Volterra Series
Yarallah Koolivand, Omid Shoaei, Ali Fotowat-Ahmadi, Ali Zahabi, Parviz Jabedar-Maralani

On-Chip 3.3V-to-1.8V Voltage Down Converter for Low-Power VLSI Chips
Qianneng Zhou

A SiGe BiCMOS Linear Regulator with Wideband, High Power Supply Rejection
Hung D. Nguyen;Benjamin J. Blalock;Suheng Chen

Optimizing Noise-Immune Nanoscale Circuits using Principles of Markov Random Fields
K. Nepal, R. I. Bahar, J. Mundy, W. R. Patterson, and A. Zaslavsky

Dynamic Instruction Schedulers in a 3-Dimensional Integration Technology
Kiran Puttaswamy, Gabriel H. Loh

Yield Enhancement of Asynchronous Logic Circuits through 3-Dimensional Integration Technology
Song Peng and Rajit Manohar

Effects of Process and Environmental Variations on Timing Characteristics of Clocked Registers
William R. Roberts and Dimitrios Velenis

Combination of Assertion and HSAT Methods for Automated Test Vector Generation
Mostafa Naderi

On Finding the Minimum Test Set of a BDD-based Circuit
Gopal Paul, Bhargab B. Bhattacharya, Ajit Pal

3:30-5:00 p.m. Session 5: Circuit Design and Modeling
Session Chair: John Lach, University of Virginia

Maximum Effective Distance of On-Chip Decoupling Capacitors in Power Distribution Grids
Mikhail Popovich, Eby G. Friedman, Michael Sotman, Avinoam Kolodny, Radu M. Secareanu

Implementation of MOSFET based Capacitors for Digital Applications
Bo Shen, Sunil P Khatri, Takis Zourntos

Integrated Low Noise Amplifier Modeling for Efficient Design Space Exploration
Tamer Ragheb, Arthur Nieuwoudt, and Yehia Massoud

3:30-5:00 p.m. Session 6: High Performance VLSI Design
Session Chair: Koushik Das, IBM

Sensitivity Evaluation of Global Resonant H-Tree Clock Distribution Networks
Jonathan Rosenfeld Eby G. Friedman

2 Gbps SerDes Design Based on IBM Cu-11 (130nm) Standard Cell Technology
Rashed Zafar Bhatti, Monty Denneau, Jeff Draper

Implementation Analysis of NoC: A MPSoC Trace-Driven Approach
Serio Tota, Mario Roberto Casu, Luca Macchiarulo

5:00-6:00 p.m. Student/Company Recruiting Session

6:30-8:30 p.m. Dinner Banquet and Invited Talk (Jeff Parkhurst, Intel)

Tuesday May 2, 2006

8:00-10:00 a.m. Session 7: Timing Optimization
Chair: Xinmiao Zhang, Case Western Reserve University

Techniques for Improved Placement-Coupled Logic Replication
Hosung (Leo) Kim, John Lillis, Milos Hrkic

A Design Flow to Optimize Circuit Delay by Using Standard Cells and PLAs
Rajesh Garg, Mario Sanchez, Kanupriya Gulati, Nikhil Jayakumar, Anshul Gupta, Sunil P Khatri

Statistical Gate Delay Calculation with Crosstalk Alignment Consideration
Bao Liu and Xu Xu

Towards a Formal Hierarchical Framework for Probabilistic Power-Performance Optimization
Joonsoo Kim, Michael Orshansky

8:00-10:00 a.m. Session 8: Testing and Noise Analysis
Session Chair: Yehia Massoud, Rice University

An Indirect Current Sensing Technique for IDDQ and IDDT Tests
Chuen-Song Chen, Jien-Chung Lo, and Tian Xia

SACI: Statistical Static Timing Analysis of Coupled Interconnects
Hanif Fatemi, Soroush Abbaspour, Massoud Pedram, Amir Ajami, Emre Tuncer

Performance Verification of High-Performance ASICs Using At-Speed Structural Test
V. Iyengar, M. Johnson, F. Woytowich, G. Grise, M. Taylor, M. Degregorio, R.W. Bassett, R. Farmer, T.E. Anemikos

Crosstalk Analysis in Nanometer Technologies
Shahin Nazarian, Ali Iranli, Massoud Pedram

10:15 a.m. -11:45 a.m. Session 9: System and Architectural-Level VLSI Design Session
Session Chair: Zhiyuan Yan, Lehigh University

Using Lin-Kernighan Algorithm for Look-up Table Compression To Improve Code Density
Talal Bonny and Joerg Henkel

FPGA Implementation of a Parallel EBCOT Tier-1 Encoder that Preserves Coding Efficiency
H. B. Damecharla K. Varma J. E. Carletta A. E. Bell

Partial Parallel Factorization in Soft-decision Reed-Solomon Decoding
Xinmiao Zhang

10:15 a.m. -11:45 a.m. Session 10: Low Power Design and Technology
Session Chair: Sanjuktha Bhanja, University of South Florida

Monotonic Static CMOS Tradeoffs in sub-100nm Technologies
Ali Bastani Charles A. Zukowski

A Power Optimized Design Methodology for Low-Distortion Sigma-Delta-Pipeline ADCs
Vahid Majidzadeh, Omid Shoaei

Perception-Guided Power Minimization for Color Sequential Displays
Wei-Chung Cheng

1:00-2:30 p.m. Poster Session 2
Session Chair: TBD

Evaluation of On-chip Networks Using Deflection Routing
Zhonghai Lu, Mingchen Zhong and Axel Jantsch

A Digit Serial Algorithm for the Integer Power Operation
Lun Li, Mitch Thornton, David W. Matula

Resource and Delay Efficient Matrix Multiplication using Newer FPGA Devices
Scott Campbell, Sunil P Khatri

Parallel Turbo-Sum-Product Decoder Architecture for Quasi-Cyclic LDPC Codes
Yongmei Dai, Zhiyuan Yan, and Ning Chen

Energy-Delay Minimization in Nanoscale Domino Logic
Bo Fu, Qiaoyan Yu, and Paul Ampadu

High Throughput Architecture for H.264/AVC Forward Transforms Block
Luciano Agostini, Sergio Bampi, Leandro Rosa, Roger Porto, José Luís Güntzel, Ivan Saraiva Silva

Hardware/Software Partitioning of Operating Systems: a Behavioral Synthesis Approach
Sathish Chandra, Francesco Regazzoni, Marcello Lajolo

A Practical Approach for Monitoring Analog Circuits
Mohamed H. Zaki, Sofiene Tahar, Guy Bois

A Non-orthogonal Clock Distribution Network and Its Performance Evaluation in Presence of Process Variations and Inductive Effects
Xu Zhang,Xiaohong Jiang and Susumu Horiguchi

A Transaction-Level Network-on-Chip Simulation Platform with Architecture-Level Dynamic and Leakage Energy Models
Jinwen Xi, Peixin Zhong

A Formal Approach for High Level Synthesis of Linear Analog Systems
Soumya Pandit, Chittaranjan Mandal, Amit Patra

Transformation Synthesis for Data Intensive Applications to FPGAs
Renqiu Huang and Ranga Vemuri

An Integrated Circuit/Behavioral Simulation Framework for Continuous-Time Sigma-Delta Analog-to-Digital Converters
Mohamed Elnozahi and Yehia Massoud

A heuristic algorithm to minimize ESOPs for multiple-output incompletely specified functions
Marios Kalathas, Dimitrios Voudouris and George Papakonstantinou

Test Generation using SAT-based Bounded Model Checking for Validation of Pipelined Processors

Heon-Mo Koo, Prabhat Mishra

An Efficient Algorithm for Partitioning Parameterized Polygons into Rectangles
I-Lun Tseng, Adam Postula

Application of a Fast Statistical Sizing Algorithm based on Second Order Conic Programming in the Industrial Microprocessor Design Flow
Murari Mani, Mahesh Sharma, Michael Orshansky

Block Alignment in 3D Floorplan Using Layered TCG
Jill H.Y. Law, Evangeline F.Y. Young and Royce L.S. Ching

Rapid Intermodulation Distortion Estimation in Fully Balanced Weakly Nonlinear Gm-C Filters using State-Space Modeling
Abdullah Celik, Zhaonian Zhang, Paul Sotiriadis

2:45 -4:45 p.m. Session 11: System and Architectural-Level Power Optimization
Session Chair: Tali Moreshet, Brown University

Selective Code/Data Migration for Reducing Communication Energy in Embedded MpSoC Architectures
Ozcan Ozturk, Mahmut Kandemir, and Mustafa Karakoy

Dynamic Voltage Scaling for Multitasking Real-Time Systems with Uncertain Execution Time
Changjiu Xian and Yung-Hsiang Lu

Low-Power Cache Organization Through Selective Tag Translation for Embedded Processors with Virtual Memory Support
Xiangrong Zhou, Peter Petrov

STV-Cache: A Leakage Energy-Efficient Architecture for Data Caches
Kimish Patel Luca Benini Enrico Macii Massimo Poncino

2:45 -4:45 p.m. Session 12: Power Aware Digital Circuits
Chair: Azeez Bhavnagarwala, IBM

A Design Methodology for Temperature Variation Insensitive Low Power Circuits
Ranjith Kumar and Volkan Kursun

Circuit Architecture for Low-power Race-free Programmable Logic Arrays
Giby Samson and Lawrence T. Clark

An Energy-Efficient Temporal Encoding Circuit Technique for On-Chip High Performance Buses
Qingli Zhang, Yizheng Ye, Jinxiang Wang

Leakage Current Starved Domino Logic
Zhiyu Liu and Volkan Kursun

4:45-5:00 p.m. Closing Remarks