2003 ACM Great Lake Symposium on VLSI

Advance Program

April 28 – 29, 2003

Monday April 28th

8:30 – 8:45 am Welcome Address

8:45 – 9:45 am Session 1: CAD
Chair: Jagan Narasimhan

s1.1 **Constructing Exact Octagonal Steiner Minimal Trees**
C. S. Coulston *(Penn State Erie, USA)*

s1.2s **Bounding the Efforts on Congestion Optimization for Physical Synthesis**
D. Pandini *(STMicroelectronics, USA),* L. T. Pileggi, A. J. Strojwas *(Carnegie Mellon University, USA)*

s1.3s **A Comprehensive High-level Synthesis System for Control-Flow Intensive Behaviors**
W. Wang, T. K. Tan, J. Luo, Y. Fei, L. Shang, K. S. Vallerio, L. Zhong,
N. K. Jha *(Princeton University, USA),* A. Raghunathan *(NEC, USA)*

10:00 am – 12:00 am Session 2: VLSI Circuits
Chair: Travis Blalock

s2.1 **Iterative Decoding In Analog CMOS**
S. Hemati, A. H. Banihashemi *(Carleton University, Canada)*

s2.2 **Design Issues in Low-Voltage High-Speed Current-Mode Logic Buffers**
P. Heydari *(University of California, USA)*

s2.3 **Optimum Wire Sizing of RLC Interconnect With Repeaters**
M. A. El-Moursy, E. G. Friedman *(University of Rochester, USA)*

s2.4s **Reduced Dynamic Swing Domino Logic**
R. Mader, I. Kourtev *(University of Pittsburgh, USA)*

s2.5s **A 5-20 GHz, Low Power FPGA Implemented by SiGe HBT BiCMOS Technology**
C. You, J.-R. Guo, R. P. Kraft, K. Zhou, M. Chu, J. F. McDonald *(Rensselaer Polytechnic Institute, USA)*

s2.6s **Interconnected Rings and Oscillators as Gigahertz Clock Distribution Nets**
M. S. Maza, M. L. Aranda *(INAOE, Mexico)*

12:00 – 1:15 pm Lunch

1:15 – 2:35 pm Session 3: Nanotechnology
Chair: Azeez Bhavnagarwala

s3.1 **Information Storage Capacity of Crossbar Switching Networks**
P. P. Sotiriadis *(John Hopkins University, USA)*

s3.2 **Exploiting Multiple Functionality for Nano-Scale Reconfigurable Systems**
P. Beckett *(RMIT University, Australia)*

s3.3s **A 0.07 µm CMOs Flash Analog-to-Digital Converter for High Speed and Low Voltage Applications**
J. Yoo, K. Choi, J. Ghaznavi *(Pennsylvania State University, USA)*

s3.4s **Modeling QCA for Area Minimization in Logic Synthesis**
N. Gergel, S. Craft, J. Lach *(University of Virginia, USA)*

2:35 – 4:00 pm Poster Session 1
Chair : Ankur Srivastava

p1.1 **Power-aware Pipelined Multiplier Design Based On 2-Dimentional Pipeline Gating**
J. Di, J. S. Yuan *(University of Central Florida, USA)*

p1.2 **Low Power VLSI Sequential Circuit Architecture Using Critical Race Control**
M. Lowy, N. Butler, R. Tinkler *(BAE Systems, USA)*

p1.3 **A Hybrid Adiabatic Content Addressable Memory for Ultra Low-Power Applications**
A. Natarajan, D. Jasinski, W. Burleson, R. Tessier *(University of Massachusetts, Amherst, USA)*

p1.4 **TEM-Cell and Surface Scan to Identify the Electromagnetic Emission of Integrated Circuits**
T. Ostermann *(University of Linz, Austria),* B. Deutschmann *(austriamicrosystems AG, Austria)*

p1.5 **MuTaTe: An Efficient Design for Testability Technique for Multiplexor based Circuits**
R. Drechsler, J. Shi, G. Fey *(University of Bremen, Germany)*

p1.6 **Cooling of Integrated Circuits Using Droplet-Based Microfluidics**
V. K. Pamula, K. Chakrabarty *(Duke University, USA)*

p1.7 **Language Emptiness Checking using MDGs**
F. Wang, S. Tahar *(Concordia University, Canada)*

p1.8 **A System-Level Methodology for Fast Multi-Objective Design Space Exploration**
G. Palermo, C. Silvano, S. Valsecchi, V. Zaccaria *(Politecnico di Milano, Italy)*

p1.9 **A Practical CAD Technique for Reducing Power/ground Noise in DSM Circuits**
A. Mukherjee, K. R. Dusety, R. Sankaranarayan *(The University of North Carolina at Charlotte, USA)*

p1.10 **RF CMOS Circuit Optimizing Procedure and Synthesis Tool**
C. Rajagopal, K. Sridhar, A. Nunez *(Syracuse University, USA)*

p1.11 **Wirelength Reduction by Using Diagonal Wire**
C. Chiang, Q. Su *(Synopsys, Inc., USA),* C.-S. Chiang *(Soochow University, Taiwan)*

p1.12 **A Fast Simulation Approach for Inductive Effects of VLSI Interconnects**

X. Qi, G. Leonhardt, D. Flees, X.-D. Yang, S. Kim, S. Mueller, H. Mau *(Sun Microsystems, Inc. USA),*
L. T. Pileggi *(Carnegie Mellon University, USA)*

p1.13 **Buffer Sizing for Minimum Energy-Delay Product by Using an Approximating Polynomial**
C. W. Kang, S. Abbaspour, M. Pedram *(University of Southern California, USA)*

p1.14 **FORCE: A Fast and Easy-To-Implement Variable-Ordering Heuristic**
F. A. Aloul, I. L. Markov, K. A. Sakallah *(University of Michigan, USA)*

p1.15 **Routing Methodology for Minimizing Interconnect Energy Dissipation**
A. Sakai, T. Yamada, Y. Matsushita *(SANYO Electric Co., Ltd., Japan),*
H. Yasuura *(Kyusyu University)*

p1.16 **Circuit Design of a Wide Tuning Range CMOS VCO with Automatic Amplitude Control**
J. Chen, B. Shi *(Tsinghua University, China)*

p1.17 **A Decoupling Technique for CMOS Strong-Coupled Structures**
L. Yang, J. S. Yuan *(University of Central Florida, USA)*

p1.18 **A Custom FPGA for the Simulation of Gene Regulatory Networks**
I. Tagkopoulos, C. Zukowski, G. Cavelier, D. Anastassiou *(Columbia University, USA)*

4:00 – 6:00 pm Session 4: VLSI Design
Chair: John Lach

s4.1 **A Novel Architecture for Power Maskable Arithmetic Units**
L. Benini *(Università di Bologna),* A. Macii, E. Macii *(Politecnico di Torino, Italy),*
E. Omerbegovic *(BullDAST s.r.l., Italy),* M. Poncino *(Università di Verona, Italy),*
F. Pro *(BullDAST s.r.l., Italy)*

s4.2 **3D Direct Vertical Interconnect Microprocessors Test Vehicle**
J. Mayega, O. Erdogan, P. M. Belemjian, K. Zhou, J. F. McDonald, Russel P. Kraft
(Rensselaer Polytechnic Institute, USA)

s4.3 **Zero Overhead Watermaking Technique for FPGA Designs**
A. K. Jain, L. Yuan, P. R. Pari, G. Qu *(University of Maryland, USA)*

s4.4s **Matrix Datapath Architecture for an Iterative 4x4 MIMO Noise Whitening Algoithm**
G. Knagge *(University of Newcastle, Australia),*
D. Garrett, S. Venkatesan, C. Nicol *(Lucent Technologies, Australia)*

s4.5s **System Level Design of Real Time Face Recognition Architecture Based on Composite PCA**
R. Gottumukkal, V. K. Asari *(Old Dominion University)*

s4.6s **Design and Modeling of a 16-bit 1.5MSPS Successive Approximation ADC with Non-binary Capacitor Array**
J. Gan *(Cirrus Logic, Inc., USA),* S. Yan, J. Abraham *(University of Texas at Austin, USA)*

6:00 – Banquet

Tuesday April 29th

8:30 – 9:45 am Session 5: VLSI Circuits
Chair: Ruchir Puri

s5.1 **Shielding Effect of On-Chip Interconnect Inductance**
M. A. El-Moursy, E. G. Friedman *(University of Rochester, USA)*

s5.2 **A Pipelined Clock-Delay Domino Carry-Lookahead Adder**
B. A. Shinkre, J. E. Stine *(Illinois Institute of Technology, USA)*

s5.3 **A Globally Asynchronous Locally Dynamic System for ASICs and SoCs**
A. Chattopadhyay, Z. Zilic *(McGill University, USA)*

s5.4s **40 MHz 0.25 µm CMOS Embedded 1T Bit-Line Decoupled DRAM FIFO for Mixed-Signal Applications**
M. I. Fuller, J. P. Mabry, J. A. Hossack, T. N. Blalock *(University of Virginia, USA)*

10:00 am – 12:00 am Session 6: CAD •
Chair: Rhett Davis

s6.1 **Design Topology Aware Physical Metrics for Placement Analysis**
S. Ramji, N. R. Dhanwada *(IBM Microelectronics, USA)*

s6.2 **A Novel Ultra-Fast Heuristic for VLSI CAD Steiner Trees**
B. Krishna *(Intel Corporation, USA),* C. Y. R. Chen *(Syracuse University, USA),*
N. K. Sehgal *(Intel Corporation, USA)*

s6.3 **Combining Wire Swapping and Spacing for Low-Power Deep-Submicron Buses**
E. Macii *(Politecnico di Torino, Italy),* M. Poncino *(Università di Verona, Italy),*
S. Salerno *(Politecnico di Torino, Italy)*

s6.4s **Clustering Based Acyclic Multi-way Partitioning**
E. S. H. Wong, E. F. Y. Young *(The Chinese University of H. K.),*
W. K. Mak *(University of S. Florida, USA)*

s6.5s **Synthesis of Continuous-Time Filters and Analog to Digital Converters by Integrated Constraint Transformation, Floorplanning and Routing**
H. Tang, H. Zhang, A. Doboli *(SUNY-Stony Brook, USA)*

s6.6s **Congestion Reduction in Traditional and New Routing Architectures**
A. R. Agnihotri, P. H. Madden *(State University of New York at Binghamton, USA)*

12:00 – 1:15 pm Lunch

1:15 – 2:15 pm Session 7: Low Power
Chair: Gang Qu

s7.1 **Simultaneous Peak and Average Power Minimization during Datapath Scheduling for DSP Processors**
S. P. Mohanty, N. Ranganathan, S. K. Chappidi *(University of South Florida, USA)*

s7.2s **Unification of Basic Retiming and Supply Voltage Scaling to Minimize Dynamic Power Consumption for Synchronous Digital Designs**
N. Chabini *(Princeton University, USA),* E. M. Aboulhamid *(Université de Montréal, Canada),*
I. Chabini *(Massachusetts Institute of Technology, USA),*
Y. Savaria *(École Polytechnique de Montréal, Canada)*

s7.3s **Branch Prediction Techniques for Low-Power VLIW Processors**
G. Palermo *(Politecnico di Milano, Italy, STMicroelectronics, Italy),* M. Sami, C. Silvano, V. Zaccaria *(Politecnico di Milano, Italy),* R. Zafalon *(STMicroelectronics, Italy)*

2:15 – 3:30 pm Poster Session 2
Chair: TBA

p2.1 **Orthogonal Code Generator for 3G Wireless Transceivers**
B. D. Andreev, E. L. Titlebaum, E. G. Friedman *(University of Rochester, USA)*

p2.2 **54x54-bit Radix-4 Multiplier based on Modified Booth Algorithm**
K. Cho, J. Park, J. Hong, G. Choi *(Samsung Electronics Co., Korea)*

p2.3 **Power-Time Flexible Architecture For GF(2k) Elliptic Curve Cryptosystem Computation**
A. A.-A. Gutub, M. K. Ibrahim *(King Fahd University of Petroleum and Minerals, Saudi Arabia)*

p2.4 **A Novel 32-bit Scalable Multiplier Architecture**
Y. Kolla *(Sun Microsystems, Inc. USA),* Y.-B. Kim *(Northeastern University, USA),*
J. Carter *(University of Utah, USA),*

p2.5 **High Throughout Overlapped Message Passing for Low Density**
Parity Check Codes
Y. Chen, K. K. Parhi *(University of Minnesota, USA)*

p2.6 **Exponential Split Accumulator for High-Speed Reduced Area**
Low-Power Direct Digital Frequency Synthesizers
E. Merlo, K-H. Baek, M. J. Choe *(Rockwell Scientific Company)*

p2.7 **Using Dynamic Domino Circuits in Self-Timed Systems**
J.-L. Yang, E. Brunvand *(University of Utah, USA)*

p2.8 **Dynamic Single-rail Self-timed Logic Structures for Power**
Efficient Synchronous Pipelined Designs
F. Grassert, D. Timmermann *(University of Rostock, Germany)*

p2.9 **Comparison of Noise Tolerant Precharge (NTP) to Conventional**
Feedback Keepers for Dynamic Logic
D. Harris, G. Breed, M. Erler, D. Diaz *(Harvey Mudd College, USA)*

p2.10 **Variable Gain Amplifier with Offset Cancellation**
A. Emira, E. Sánchez-Sinencio *(Texas A&M University, USA)*

p2.11 **Repeater and Current-sensing Hybrid Circuits for On-chip Interconnects**
A. Maheshwari, W. Burleson *(University of Massachusetts, Amherst, USA)*

p2.12 **A Slew Rate Enhancement Technique for Operational Amplifiers**
based on a Tunable Active Gm-based Capacitance Multiplication Circuit
R. Suryanarayan, A. Gupta, T. N. Blalock *(University of Virginia, USA)*

p2.13 **A Dual band CMOs VCO with a Balanced Duty Buffer**
Y. C. Han *(Samsung Electronics Co., Korea),* K. Kim, J. Kim,
K. S. Yoon, J. Chen, B. Shi *(Inha University, Korea)*

p2.14 **New Approach to CMOS Current Reference with Very Low**
Temperature Coefficient
J. Chen, B. Shi *(Tsinghua University, China)*

p2.15 **Noise Tolerant Low Voltage XOR-XNOR for Fast Arithmetic**
M. Elgamel, S. Goel, M. Bayoumi *(University of Louisiana at Lafayette, USA)*

3:30 – 4:45 pm Session 8: Testing
Chair: TBA

s8.1 **On Automatic Generation of RTL Validation Test Benches**
Using Circuit Testing Techniques
I. Ghosh *(Fujitsu Laboratories of America, USA),* S. Ravi *(NEC Laboratories of America, USA)*

s8.2s **A Highly Regular Multi-Phase Reseeding Technique for Scan-based BIST**
E. Kalligeros, X. Kavousianos *(University of Patras, Greece),*
D. Nikolos *(Computer Technology Institute, Greece)*

s8.3s **Coefficient-Based Parametric Faults Detection in Analog Circuits**
Z. Guo *(New Jersey Institute of Technology, USA)*

s8.4s **Mixing ATPG and Property Checking for Testing HW/SW Interfaces**
A. Fin, F. Fummi, G. Pravadelli *(University of Verona, Italy)*

4:45 – 5:00 pm Closing Remarks